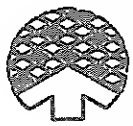
Databook

Local Bus VGA Graphics Controller

OTI-087

NEW



OAK TECHNOLOGY, INC.™

System Solutions in Silicon

OTI-087X Addendum to the Databook

This Addendum describes changes to the OTI-087 February 1993 databook for OTI-087X parts. The OTI-087X currently does not support the RAS only refresh DRAM, 260's type DRAM and integrated feature connector support.

Page	Description
1	Disregard the reference to RAS only refresh in the feature list. This is currently not supported.
8	Disregard CAS0n, CAS1n, CAS2n and CAS3n signals on the Operational Block Diagram.
13	This MD interface is not supported with this OTI-087 revision.
16	Disregard CAS0n, CAS1n, CAS2n and CAS3n signals on the Memory Mapping Configuration.
25	EPDATA should be DCn under the OTI-087 (LB386/486) column.
28	Pin 99 on OTI-087 (LB 386/486) should be DCn.
37	Extended Register 8, bits 6, 1, 0 should be as below. Also, pin 99 does not apply.

Bits 6, 1, 0	Pin 19	Pin 20
1 0 1	EPCLK	EPDATA
110	EPCLK	EPDATA

Bit 7 Reserved.

60 See attached for new Local Bus Schematics.

OTI-087 Drivers List

esolution	640x400		640x480					800x600			1024x768				768x1024	1280x1024	1280x1K		Text
olors	32K	64K	16	256	256-linear	32K	64K	16	256	256-linear	4	16	256	256-linear	16	16	256*	256-linear*	132x25,43,60
RIVERS:																			
utoCAD 2.62								x											
utoCAD 9/10/11/12			x	x				x	x		x	x	x		x	x			
utoShade 1.0/2.0	x			x		x			x				x						
dvance 4.0/4.1								x				x			x				
ramework II			x					x											132x25,43,60
ramework III			x					x											132x25,43,60
EM/3 3.1								x			x	x			x				
otus123 2.0x			x					x											132x25,43
otus 123 2.2								x			x	x			x				132x25,43,60
otus 123 3.0/3.1								x			x	x			x				resolution dependent
rcad 4.0												x							
S/2 2.1				x					x				x						
-CAD 4.5								x				x			x				
entura 1.1								x											
entura 2.0								x			x	x			x				
ersaCAD 6.0				x				x	x		x	x							
ersaCAD/386 6.0				x				x	x		x	x							
ESA TSR				x				x	x			x							132x25,43,60,80x60
ordPerfect 5.0								x											
ordPerfect 5.1								x			x	x			x				132x25,43,60
indows 3.1	x	x		x	x	x	x	x	x	x		x	x	x	x	x	x	x	
indows NT 3.1				x				x	x			x	x		x	x	x		

These resolutions are only supported by OTI-087 due to the requirement of 2Mbytes of video memory.

Preface

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February 1993

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OTI-087 LOCAL BUS VGA CONTROLLER

Description

The OTI-087 is a highly integrated, single chip Local Bus VGA Controller compatible with the IBM VGA standard. The OTI-087 offers a low-cost implementation for 24-bit color at a resolution of 640x480 while being capable of high resolutions including 1024x768 non-interlaced with 256 colors and 1280x1024 interlaced with 256 colors. The OTI-087 is completely compatible with the IBM VGA standard and implements all registers and data paths while providing improved performance and additional functionality. Especially attractive for motherboard applications, the OTI-087 supports high speed local bus implementations for cost-effective high performance graphics.

Features

- IBM VGA compatible graphics controller with resolutions up to:
  - 1024x768, 256 colors Non-Interlaced
  - 1280x1024, 256 colors Interlaced
  - 640x480, 16.8 million colors (24-bit)
- 100% Hardware and BIOS compatible with IBM's VGA
- Supports up to 2 MBytes of memory:
  - 2, 4 or 8 64K X 16 DRAMs
  - 2, 4, 8 or 16 256K X 4 DRAMs
  - 2 or 4 256K X 16 DRAMs
  - 2 or 4 512K X 8 DRAMs
- Hardware cursor (64x64 2 bits/pixel)
- Integrated feature connector support
- Write cache for high speed local bus implementation
- Read cache optimizes memory bandwidth usage
- Integrated zero wait state AT bus performance
- Supports 8, 16, or 32-bit memory interface with fast page operation
- Supports CAS before RAS and RAS only refresh
- Supports VESA-standard high vertical refresh rates of 72 Hz for flicker-free displays
- Up to 80 MHz maximum video clock rate
- Complete linear addressability in protected mode
- Packed pixel format for 256 color modes
- Foreground/background color expansion registers for fast text output
- 16-bit graphics latch for true 16-bit operations in planar modes
- Special 256 color pattern and fill modes increase performance
- Supports 132 column text
- Integrated bus interface for PC/XT/AT and local bus implementations
- Supports portrait monitors
- True 16-bit I/O read/write operations
- EEPROM support provides switchless configurations

Supported Screen Formats

The OTI-087 not only supports all standard IBM VGA modes, but the following extended modes as well.

Mode	Resolution	Colors	Font	Alpha Format	Dot Clk(MHz)	H-freq(KHz)	V-freq(Hz)	Non-Interlaced	Video Memory	VESA
12h*	640 x 480	16	8 x 16	80 x 30	25.175	31.50	60	Yes	256K	N/A
12h	640 x 480	16	8 x 16	80 x 30	31.500	37.86	72	Yes	256K	Standard
4Eh*	80 x 60	16	8 x 8	80 x 60	25.175	31.50	60	Yes	256K	N/A
4Fh*	132 x 60	16	8 x 8	132 x 60	40.000	31.50	60	Yes	256K	N/A
50h*	132 x 25	16	8 x 14	132 x 25	40.000	31.50	70	Yes	256K	N/A
51h*	132 x 43	16	8 x 8	132 x 43	40.000	31.50	70	Yes	256K	N/A
52h*	800 x 600	16	8 x 16	100 x 37.5	36.000	35.16	56	Yes	256K	Mfg. G.L.
52h	800 x 600	16	8 x 16	100 x 37.5	40.000	37.88	60	Yes	256K	Mfg. G.L.
52h	800 x 600	16	8 x 16	100 x 37.5	50.000	48.08	72	Yes	256K	Standard
53h*	640 x 480	256	8 x 16	80 x 30	25.175	31.50	60	Yes	512K	N/A
53h	640 x 480	256	8 x 16	80 x 30	31.500	37.86	72	Yes	512K	Standard
54h*	800 x 600	256	8 x 16	100 x 37.5	36.000	35.16	56	Yes	512K	Mfg. G.L.
54h	800 x 600	256	8 x 16	100 x 37.5	40.000	37.88	60	Yes	512K	Mfg. G.L.
54h	800 x 600	256	8 x 16	100 x 37.5	50.000	48.08	72	Yes	512K	Standard
55h	1024 x 768	4	8 x 16	128 x 48	44.900	35.52	87	No	256K	N/A
55h*	1024 x 768	4	8 x 16	128 x 48	65.000	48.36	60	Yes	256K	Mfg. G.L.
55h	1024 x 768	4	8 x 16	128 x 48	78.000	56.69	70	Yes	256K	Standard
55h	1024 x 768	4	8 x 16	128 x 48	78.000	58.04	72	Yes	256K	N/A
56h	1024 x 768	16	8 x 16	128 x 48	44.900	35.52	87	No	512K	N/A
56h*	1024 x 768	16	8 x 16	128 x 48	65.000	48.36	60	Yes	512K	Mfg. G.L.
56h	1024 x 768	16	8 x 16	128 x 48	78.000	56.69	70	Yes	512K	Standard
56h	1024 x 768	16	8 x 16	128 x 48	78.000	58.04	72	Yes	512K	N/A
57h	768 x 1024	16	8 x 16	96 x 64	44.900	46.77	87	No	512K	N/A
57h*	768 x 1024	16	8 x 16	96 x 64	65.000	59.74	55	Yes	512K	N/A
58h*	1280 x 1024	16	8 x 16	160 x 64	78.000	48.75	87	No	1M	N/A
59h[2]	1024 x 768	256	8 x 16	128 x 48	44.900	35.52	87	No	1M	N/A
59h*[1]	1024 x 768	256	8 x 16	128 x 48	65.000	48.36	60	Yes	1M	Mfg. G.L.
59h[1]	1024 x 768	256	8 x 16	128 x 48	78.000	56.69	70	Yes	1M	Standard
59h[1]	1024 x 768	256	8 x 16	128 x 48	78.000	58.04	72	Yes	1M	N/A
5Ah*[2]	640 x 480	64K	8 x 16	80 x 30	50.000	31.50	60	Yes	1M	N/A
5Ah[1]	640 x 480	64K	8 x 16	80 x 30	63.000	37.86	72	Yes	1M	Standard
5Bh*	640 x 400	32K/64K	8 x 16	80 x 25	50.000	31.50	70	Yes	512K	N/A
5Ch*[2]	640 x 480	32K	8 x 16	80 x 30	50.000	31.50	60	Yes	1M	N/A
5Ch[1]	640 x 480	32K	8 x 16	80 x 30	63.000	37.86	72	Yes	1M	Standard
5Dh*[1]	800 x 600	32K	8 x 16	100 x 37.5	78.000	37.50	60	Yes	1M	Mfg. G.L.
5Eh*	1280 x 1024	256	8 x 16	160 x 64	78.000	48.75	87	No	2M	N/A
5Fh*	640 x 480	16.8M	8 x 16	80 x 30	78.000	31.55	60	Yes	1M	N/A
60h*[1]	800 x 600	64K	8 x 16	100 x 37.5	78.000	37.50	60	Yes	1M	Mfg. G.L.
61h*	640 x 400	256	8 x 16	80 x 25	25.175	31.50	70	Yes	256K	N/A

Software Driver Support

Oak Technology was the first graphics company to promote the importance of the hardware-software driver relationship. Thus, Oak is committed to providing customers with the most powerful software drivers. Oak's software driver support includes the fastest drivers available for popular applications including:

AutoCAD
AutoShade
CADvance
GEM
Lotus 1-2-3/Symphony
P-CAD
OS/2
OS/2 Presentation Manager
VersaCAD
VESA BIOS Extensions
WordPerfect/DrawPerfect/PlanPerfect
Ventura
UNIX (ISC & SCO)
OrCAD
EasyCAD/FastCAD
Microsoft Windows
Wordstar

Display Memory Interface

The OTI-087 supports 64Kx16, 256Kx4, 256Kx16, and 512Kx8 DRAM devices. The OTI-087 provides all the necessary control signals and address and data lines to access the video memory in page mode. The control signals can be programmed to optimize memory cycles for a given memory type and speed for a specific memory clock. The maximum video buffer size is 2Mbytes when used with 256Kx4, 256Kx16 or 512Kx8 DRAMs and 1Mbyte when used with 64Kx16 DRAMs. Minimum configuration is 256Kbytes when used with 64Kx16 or 256Kx4 DRAMs and 1Mbyte when used with 512Kx8 or 256Kx16 DRAM. The video buffer can be addressed through either a programmable linear address range above 1M or through the conventional video address (A0000 to $BFFFF_H$) using the segment registers.

Clock Interface

Up to 16 external video clock frequencies can be selected by four programmable clock select pins. Video clock frequencies up to 80 MHz can be supported. When implemented with the OTI-068 Dual Clock Generator, the OTI-087 can select sixteen pixel clock frequencies providing support for both conventional and flicker-free VESA vertical refresh rates without any hardware switches. The OTI-068 also supports three memory clock frequencies which can be selected through hardware configuration to optimize performance with a wide variety of DRAM types and speeds.

System Bus Interface

The system bus of the OTI-087 can be connected to the PC system in three different configurations: on-board local bus, add-on local bus and on-board AT bus. The OTI-087 can also be connected to the AT bus. The mode of operation is defined by the **Configuration Register 1** status, set through the MD[7:0] bus during reset time.

System Configuration	Bit 2	Bit1
Local Bus	0	0
Local Bus Add-on	0	1
On-board AT	1	0
Add-on AT	1	1

Local Bus Interface

In Local Bus configuration, the OTI-087 can interface to the 80286, 80386SX, 80386DX, and 80486 CPUs. Configuration of the OTI-087 for the proper CPU local bus is accomplished through the ADSn pin and the **Configuration Register 2** as detailed in the table below. **Configuration Register 2** is set through the MD[15:8] bus during reset.

Local Bus Mode	ADSn	Bit 1	Bit 0
80286 Local Bus	0	0	0
80386SX Local Bus	1	0	0
80386DX Local Bus	1	0	1
80486 Local Bus	1	1	0

To ensure the above detection scheme will operate properly, a weak pull-down resistor should be connected to the ADSn pin of the OTI-087. Since the 80286 processor does not have ADSn, this signal should remain low during reset in 80286 designs. For proper operation in 80386 and 80486 processor designs, this signal will be reset high.

OTI-087 Local Bus with 80286 and 80386SX Processors

The local bus interface of the OTI-087 provides an optimal implementation for 80286 and 80386SX designs which use Oak Technology's OTI-020 system chipset. An implementation of the OTI-087 with the OTI-020 requires no external logic for local bus interface.

The video space of the OTI-087/OTI-020 local bus video system is defined by the VIDEO1 register (port $1F_H$ index 5). When any one of the video segments in this register is enabled, the OTI-020 system chipset generates a video cycle to the external bus and terminates the CPU cycle. If the video segments are disabled, the local bus OTI-087 will terminate the CPU cycle. Graphics Register $3DF_H$, Index 6 only affects the access to video memory and has no effect on the generation of SRDY. At system boot-up time, the system will scan for the presence of any off-board memory which occupies the A0000-$BFFFF_H$ range. If off-board video memory is detected, the VIDEO1 register (present in both the OTI-020 system chipset and the OTI-087) will be programmed so that the local bus system responds to all the memory in A0000-$BFFFF_H$, excluding the enabled segments in the VIDEO1 register.

The OTI-087 supports 16-bit, zero-wait-state CPU memory operations through the CPU local bus. The OTI-087 uniquely employs both a read cache and a write cache to achieve zero-wait-state memory operations for local bus speeds up to 33 MHz. During the CPU memory cycle, the OTI-087 interprets the status lines (WRn and DCn) and the address CA19-CA17 (101_H) gated with the VIDEO1 register to generate a local bus memory cycle. If the requested data is already inside the OTI-087 read cache during a memory read, SRDY is returned in the next CPU clock, thus a zero-wait-state memory cycle. Otherwise, SRDY is not returned until the data is read from the video memory and driven out to the bus. For writes to video memory, a memory write request is stored inside the write cache and SRDY is returned in the next CPU clock for a zero-wait-state memory cycle. If either the write cache is full or the write address does not share the same cache page as the previous write, then SRDY is not returned until the data is actually written to the video memory.

The OTI-087 supports 16-bit I/O access and 8-bit memory access for DMA and MASTER cycles. During a DMA or MASTER cycle, the OTI-087 receives I/O and memory commands from the AT-bus and transfers data to the local SD bus as if it were a 16-bit device. In this case, both SD[7:0] and SD[15:8] are driven with the same data. During I/O cycles, the OTI-087 receives commands from the AT-bus and transfers data on the local bus. The system chipset is responsible for routing the address and data to and from the AT-bus.

80386DX and 80486 Local Bus

This section refers to the 80386DX/80486 block diagrams following this section. The OTI-087 requires four buffers (A,B,E,F in the diagram) and 1 PAL to interface with the 80386DX CPU. Two additional buffers (C,D in the diagram) are required to interface with the 80486 CPU. The PAL is used to decode the upper address of the CPU and generate the CPU address 0,1 and the CPUBHEn signal for the OTI-087. The A,B buffers are used to interface the OTI-087 data bus to AT-data bus while the C,D,E,F buffers are used to interface the OTI-087 data bus to the CPU data bus.

During I/O, DMA or MASTER cycles, the OTI-087 receives bus commands from the AT-bus. During a CPU memory cycle, the OTI-087 will use the CPUA0/A1/BHEn signals to execute the cycle. The LBSELn signal is the protocol between the system chipset and the OTI-087 to determine ownership of the current memory cycle. If the current memory cycle belongs to the OTI-087 address space, the OTI-087 forces the LBSELn signal low at the beginning of T2 and terminates the cycle with SRDY. If the current memory cycle does not belong to the OTI-087 address space the system chipset should terminate the cycle. In 80386DX and 80486 configura-

tions, there are two reset signals connected to the OTI-087. The RSET signal is connected to the system reset and the CPURESET is connect to the CPU reset. The OTI-087 uses the CPURESET signal to synchronize the internal clock and uses the RSET signal to reset the OTI-087. If the system chipset does not drive a valid address to the CPU bus during DMA or MASTER cycles, then more huffers are necessary to route the address to the CPU hus. Buffer G in 80386DX/80486 block diagrams illustrate this implementation.

Summary of Performance Features

The OTI-087 implements all of the standard state-of-the-art features for high speed frame-buffer graphics controllers. These standard features include independent memory and pixel clocks, support for high refresh displays, highly integrated bus interfaces, and true 16-bit I/O read/write operations. In addition, the OTI-087 implements several next generation features which advance the state-of-the-art in graphics frame-buffer technology.

High Speed Local Bus

The OTI-087 is one of the first PC graphics controllers designed from the ground up for motherboard architectures implementing direct CPU interfaces to the video controller. The local control signals of the OTI-087 provide accelerated system to video memory transfers. Timing overhead is also reduced. To take advantage of the high transfer rates, the OTI-087 implements the most features of any frame-buffer controller for assisting CPU-hased graphics operations.

Hardware Cursor

The Hardware Cursor (HC) increases the overall graphics performance by reducing the need for the CPU to redraw the cursor during each update. Also, the image under the cursor does not have to be updated hy software when the cursor is moved. Lastly, the cursor appears continuously and is more responsive.

Write Cache

When writing to the OTI-087, hoth data and address are latched from the system bus and the zero-wait-state signal is activated, unless the cache is full. When implemented in the AT-bus configuration, the OTI-087 will exhibit zero-wait-state performance in lower resolution/color and planar modes. In higher resolution, the percentage of zero-wait cycles will decrease for packed pixel modes with increasing bus speed, resolution, color depth, and vertical refresh.

Read Cache

The read cache of the OTI-087 was designed to accelerate bitblt functions. When executing block moves, often the next operation requires a read from an adjacent memory location. In this case, the desired data will he in the read cache and the operation can execute without waiting for a memory cycle.

Linear Addressability

In extended video modes where more than 256Khytes of video buffer are required, the video driver must perform segment checking and address calculation to determine a given pixel's location in video memory. At programmable addresses above 1 Mbyte, the OTI-087 provides linear memory mapping thereby eliminating segment checking. Linear addressing speeds all functions when running applications in protected-mode.

Foreground/Background Color Expansion

In packed pixel modes, the output of simple text becomes more cumbersome. To reduce the number of individual memory operations required, the OTI-087 contains foreground/background color expansion registers which allow eight consecutive bytes to be expanded from one byte containing the foreground or background bits. A pixel masking capability is also implemented to be able to leave specified pixels unchanged. This also speeds masked bitblt functions.

256 Color Patterns and Fills

For packed pixel modes, the OTI-087 provides a pattern register for defining patterns and expanding the color information from either OTI-087 registers or CPU data. This allows fast pattern fill.

16-bit Graphics Latch

Most currently available VGA controllers only allow for byte operations in many cases. The OTI-087, as with previous generations of Oak VGA controllers, provides true 16-bit move operations in all situations. Relative to other VGA controllers, this is particularly useful for pattern blts and source copy bitblts where MOVSW instructions can replace MOVSB instructions.

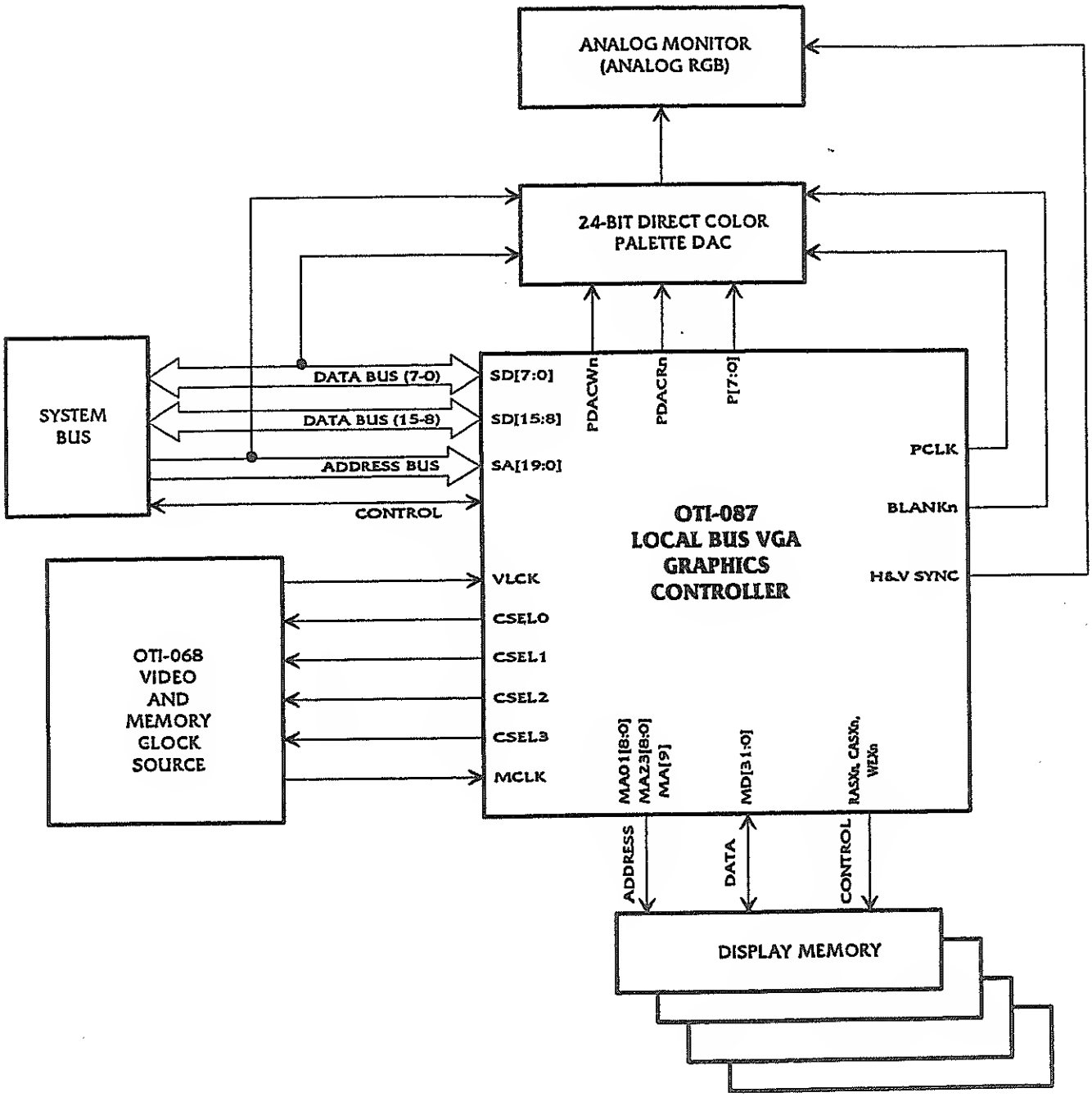
EEPROM Support

In a VGA-based video system, certain configuration information must be available to the video BIOS. It is common practice on many video adapter boards to use jumpers or switches to provide the proper settings. These switch settings can cause confusion for the consumer. To simplify the situation, the OTI-087 provides support for a serial EEPROM which stores the specific configuration information. The configuration is done through software, eliminating all jumpers and switches.

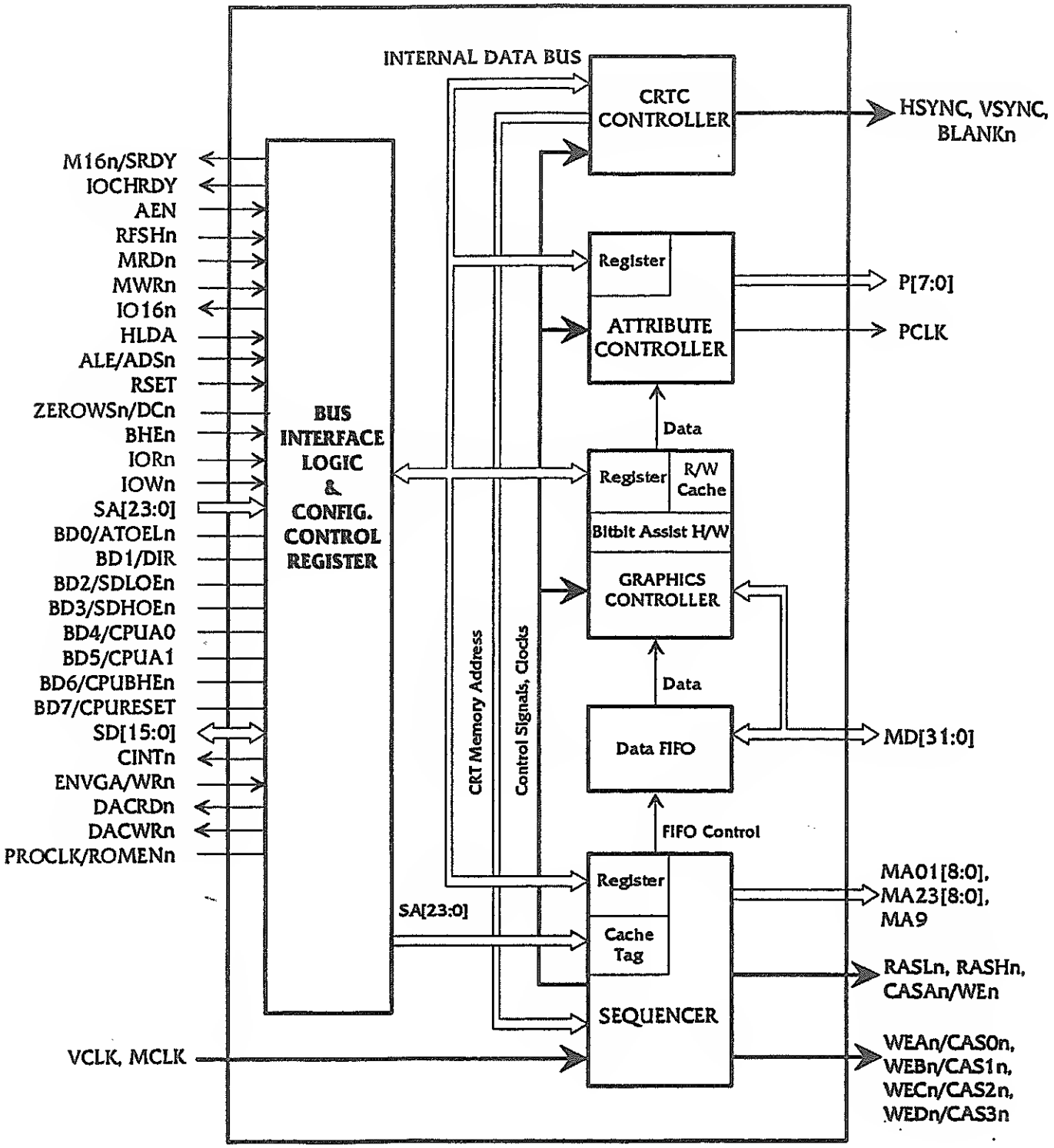
80 Mbyte/sec Video

Fixed clock rates to 80 MHz allow the OTI-087 to offer vertical refresh rates at 1024x768 that exceed the VESA standard of 70 Hz for high vertical refresh displays. Depending on the capabilities of the monitor, the OTI-087 can support up to 1024x768 with 256 colors at a 76 Hz vertical screen refresh.

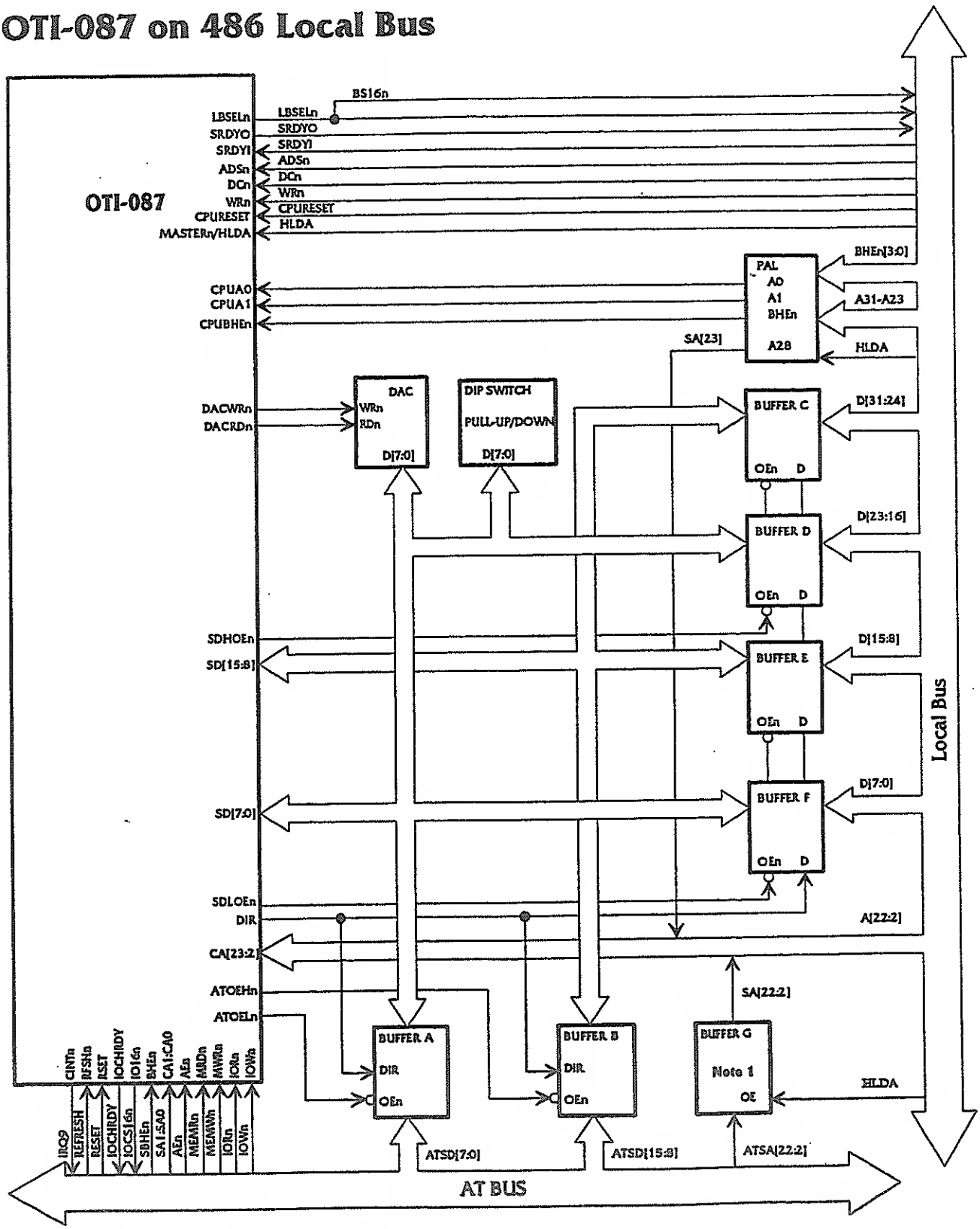
OTI-087 System Block Diagram



OTI-087 Operational Block Diagram

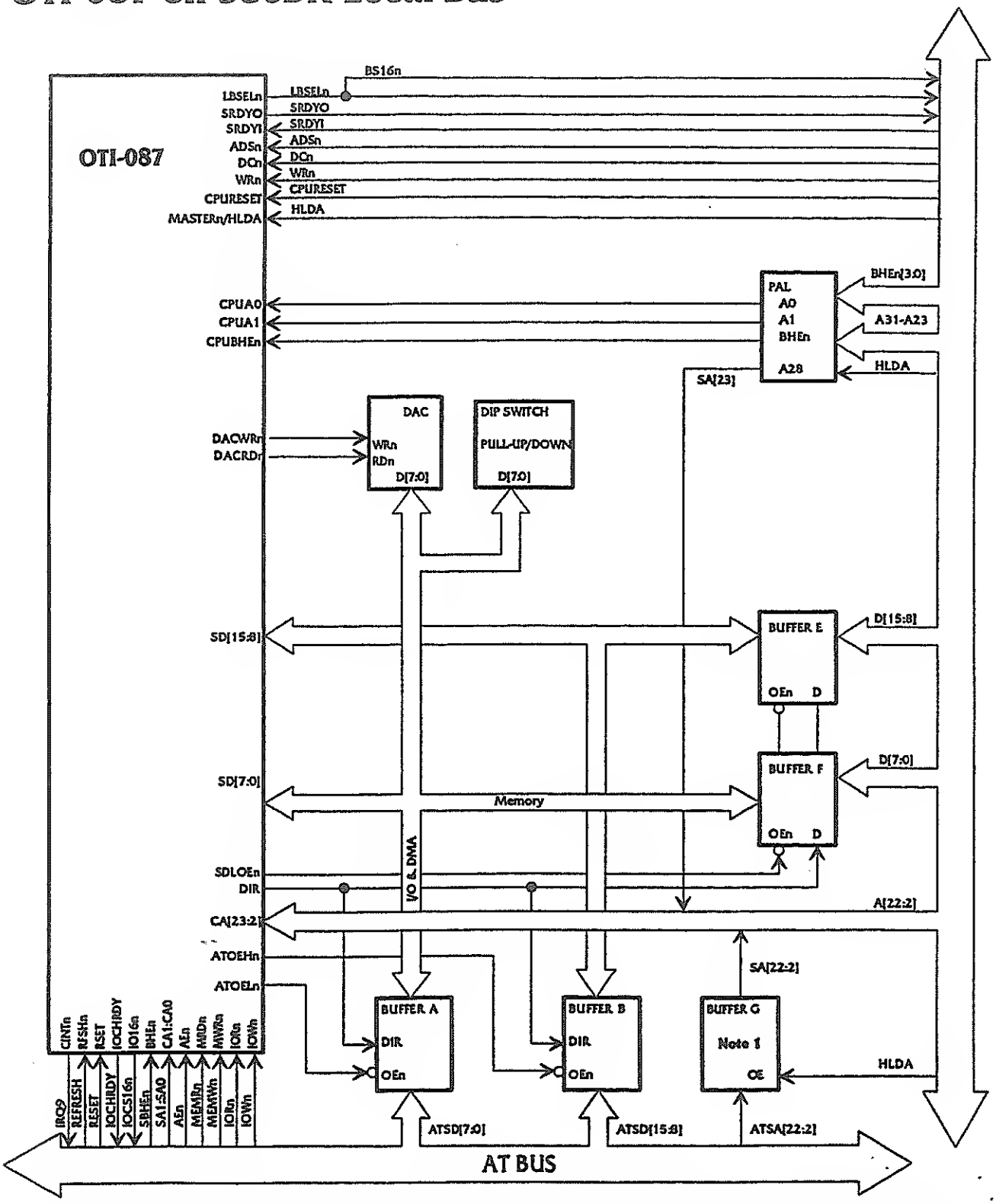


OTI-087 on 486 Local Bus



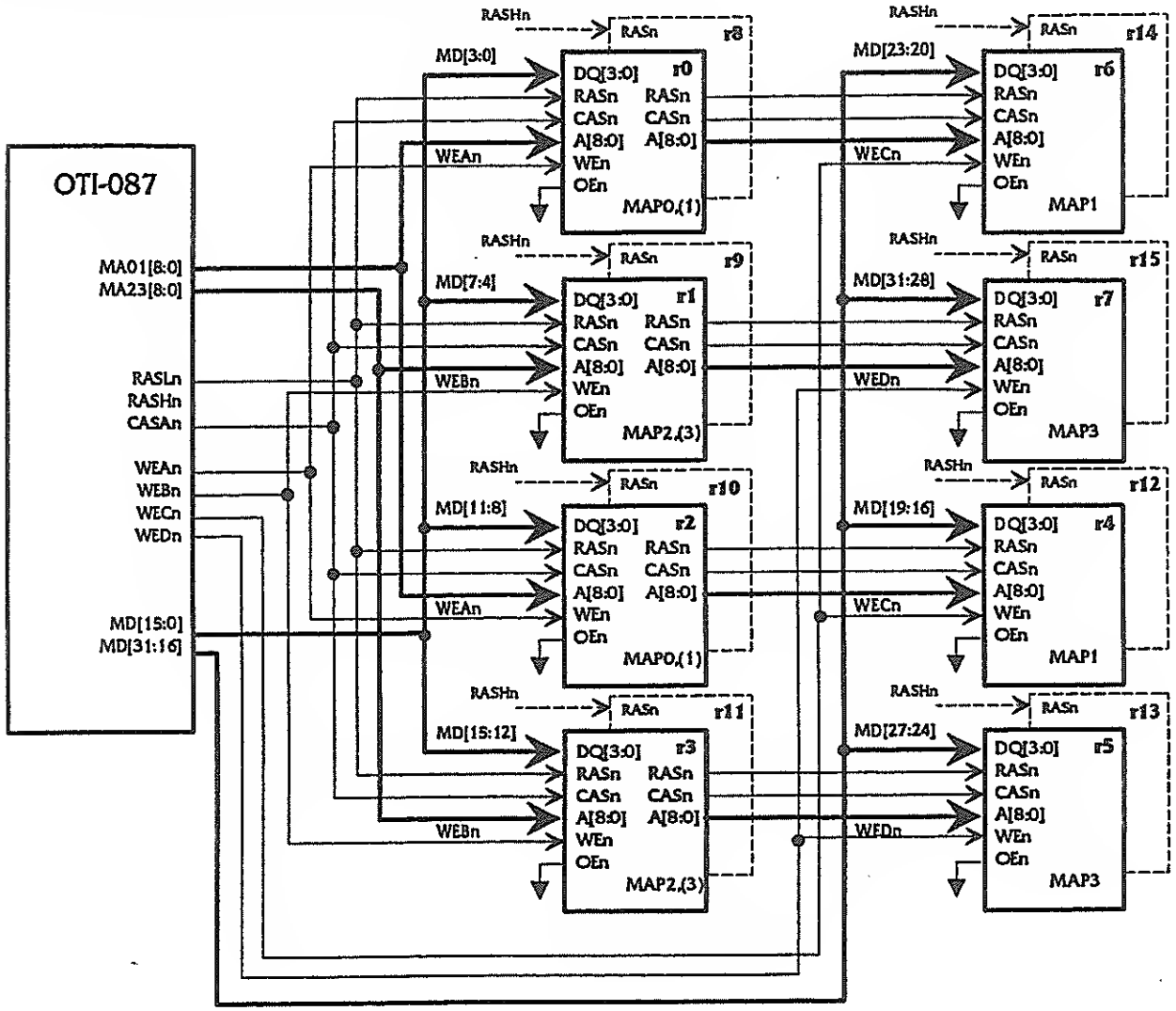
Note 1: Buffer G is needed only if the system chipset does not route back these address signals during DMA/Master cycles.

OTI-087 on 386DX Local Bus

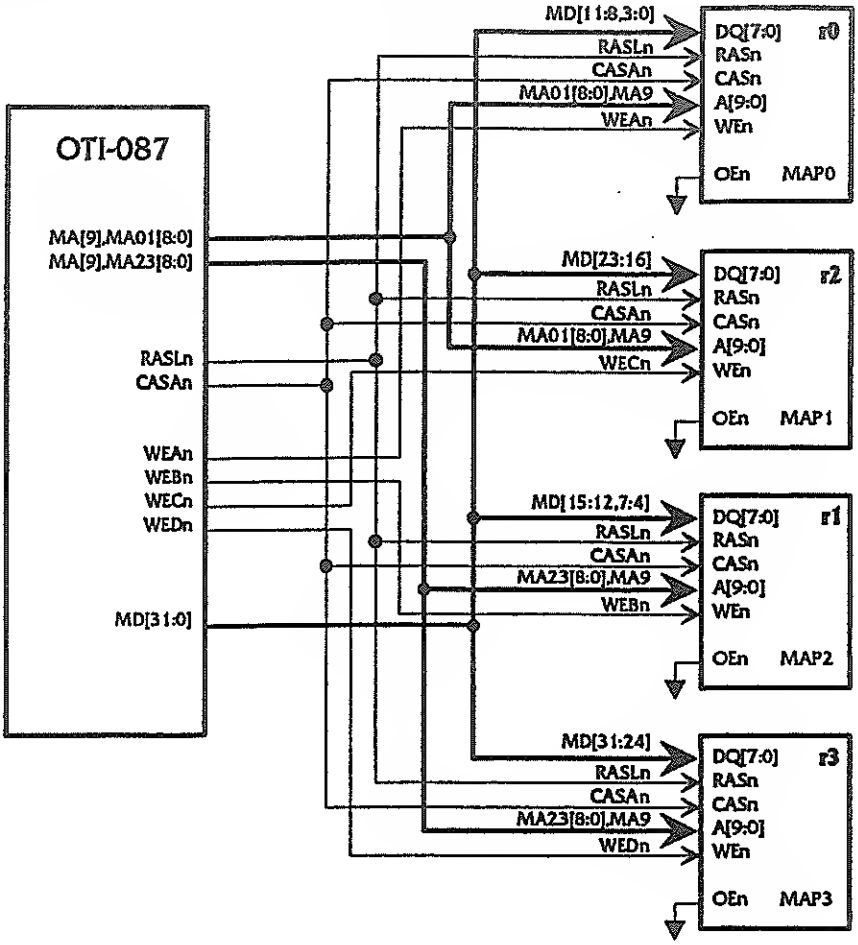


Note 1: Buffer G is needed only if the system chipset does not route back these address signals during DMA/Master cycles.

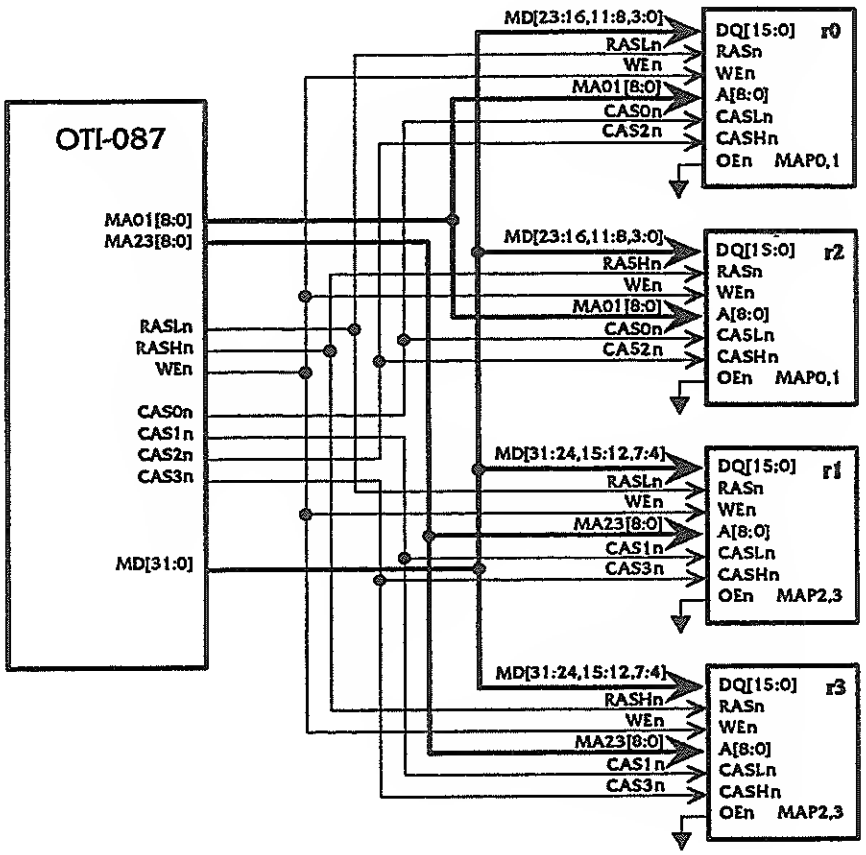
MD Interface for 256K x 4 DRAMs



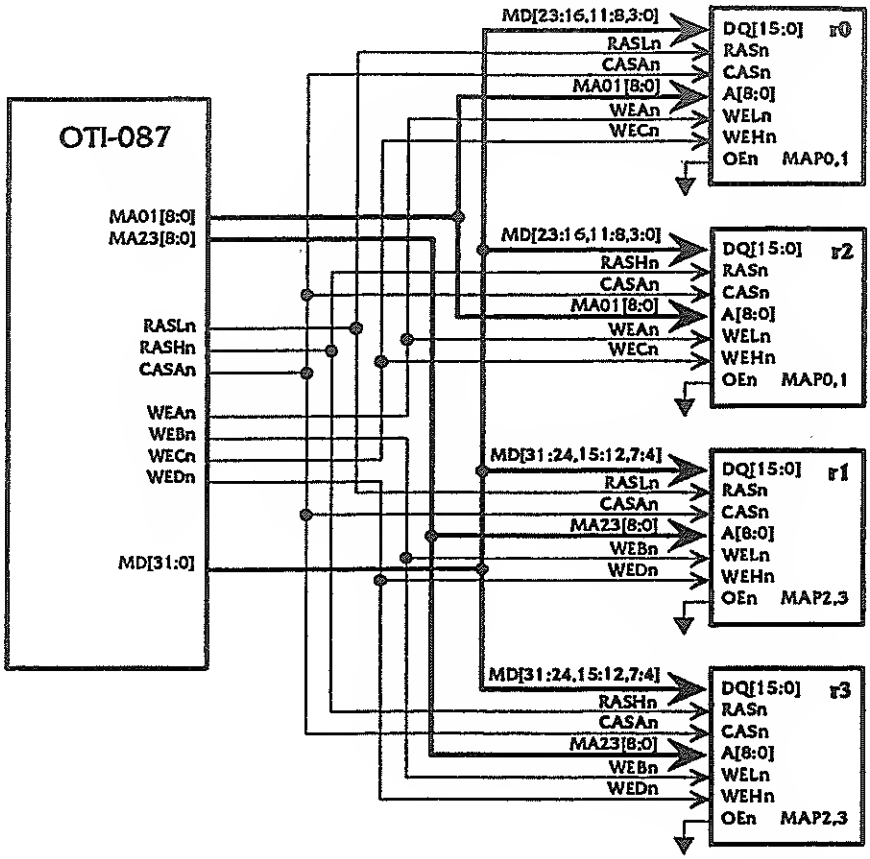
MD Interface for 512K x 8 DRAMs



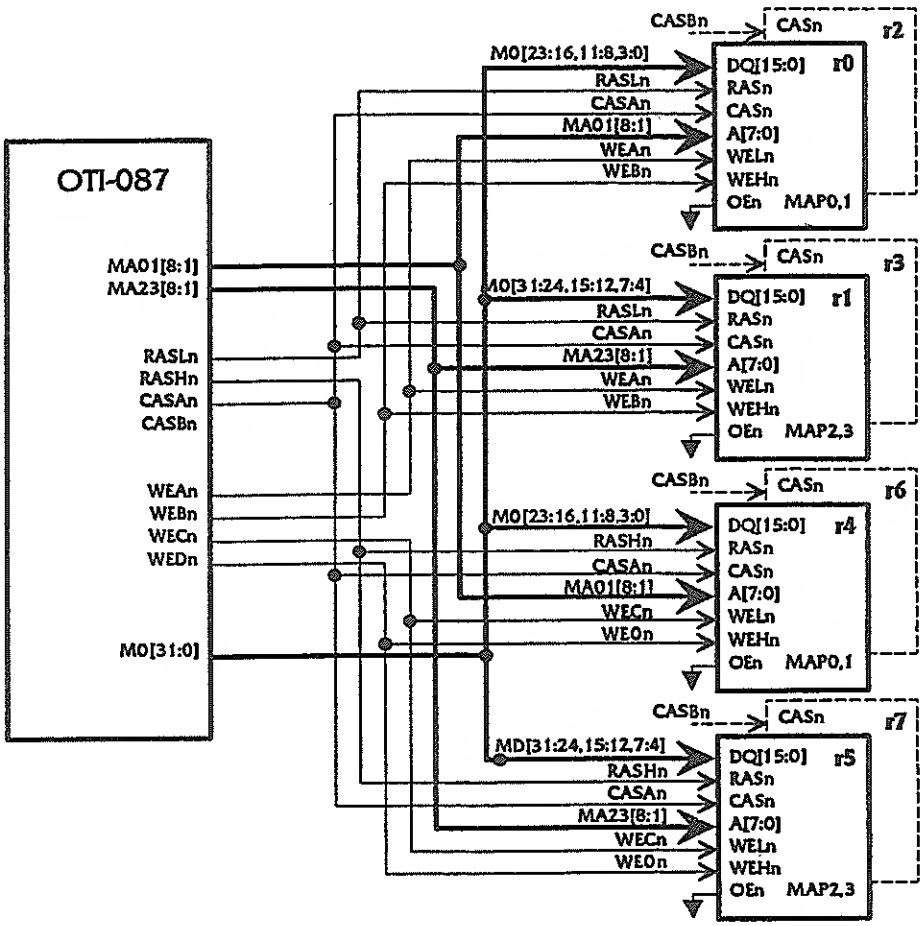
MD Interface (260) for 256K x 16 DRAMs



MD Interface (270) for 256K x 16 DRAMs



MD Interface for 64K x 16 DRAMs



Memory Mapping Configuration

	256Kx4 (2) MD8	256Kx4 (4) MD16	512Kx8 (2) MD16	256Kx4 (8 or 16) MD32	256Kx16 (2 or 4) MD32	512Kx8 (4) MD32	64Kx16 (2, 4, or 8) MD32
MAP0	MD[3:0] r0	MD]11:8,3:0] r2,0	MD[11:8,3:0] r0	MD]11:8,3:0] r2,0 (10,8)	MD[11:8,3:0] r2,0 (2)	MD[11:8,3:0] r2,0	MD[11:8,3:0] r2.0 (2) (4,6)
MAP1	MD[3:0] r0	MD[11:8,3:0] r2,0	MD]11:8,3:0] r0	MD]23:16] r6,4 (14,12)	MD[23:16] r0 (2)	MD[23:16] r2	MD[23:16] r0 (2) (4,6)
MAP2	MD[7:4] r1	MD[15:12, 7:4] r3,1	MD[15:12, 7:4] r1	MD[15:12, 7:4] r3,1 (11,9)	MD[15:12, 7:4] r1 (3)	MD[15:12, 7:4] r1	MD]15:12, 7:4[r1 (3) (5,7)
MAP3	MD[7:4] r1	MD[15:12, 7:4] r3,1	MD[15:12, 7:4] r1	MD]31:24] r7,5 (15,13)	MD[31:24] r1 (3)	MD[31:24] r3	MD[31:24] r1 (3) (5,7)
RAM0 (8)	MD[3:0]	MD[3:0]	MD]11:8,3:0]	MD]3:0]	MD[23:16, 11:8,3:0]	MD[11:8,3:0]	MD[23:16, 11:8,3:0]
RAM1 (9)	MD[7:4]	MD[7:4]	MD[15:12, 7:4]	MD]7:4]	MD]31:24, 15:12,7:4]	MD[15:12, 7:4]	MD[31:24, 15:12,7:4]
RAM2 (10)	Not Applicable	MD[11:8]	Not Applicable	MD[11:8]	MD]23:16, 11:8,3:0]	MD[23:16]	MD[23:16, 11:8,3:0[
RAM3 (11)	Not Applicable	MD[15:12[	Not Applicable	MD[15:12]	MD[31:24, 15:12,7:4]	MD[31:24]	MD[31:24, 15:12,7:4[
RAM4 (12)	Not Applicable	Not Applicable	Not Applicable	MD]19:16]	Not Applicable	Not Applicable	MD[23:16, 11:8,3:0]
RAM5 (13)	Not Applicable	Not Applicable	Not Applicable	MD]27:24]	Not Applicable	Not Applicable	MD]31:24, 15:12,7:4]
RAM6 (14)	Not Applicable	Not Applicable	Not Applicable	MD[23:20]	Not Applicable	Not Applicable	MD[23:16, 11:8,3:0]
RAM7 (15)	Not Applicable	Not Applicable	Not Applicable	MD[31:28]	Not Applicable	Not Applicable	MD[31:24, 15:12,7:4]
RASLn	r0,1	r0,1,2,3	r0,1	r0,1,2,3, 4,5,6,7	r0,1	r0,1,2,3	r0,1,2,3
RASHn /MA9	N.C.	N.C.	r0,1	r8-18	r2,3	r0,1,2,3	r4,5,6,7
CASAn /WEn	r0,1	r0,1,2,3	r0,1	r0-15	r0,1,2,3	r0,1,2,3	r0,1,4,5
WEAn /CAS0n	r0 MAP0.1	r0.1 MAP0,1	r0 MAP0.1	r0,2,8,10 MAP0	r0,2 (WELn/CASLn) MAP0	r0 MAP0	r0,2,4.6 (WELn) MAP0
WEBn /CAS1n	r1 MAP2,3	r2,3 MAP2,3	r1 MAP2.3	r1,3,9,11 MAP2	r1,3 (WELn/CASLn) MAP2	r1 MAP2	r1,3,5,7 (WELn) MAP2
WECn /CAS2n	N.C.	N.C.	N.C.	r4,6,12,14 MAP1	r0,2 (WEHn/CASHn) MAP1	r2 MAP1	r0,2,4,6 (WEHn) MAP1
WEDn /CAS3n	N.C.	N.C.	N.C.	r5,7,13,15 MAP3	r1,3 (WEHn/CASHn) MAP3	r3 MAP3	r1,3,5,7 (WEHn) MAP3
MA01 [0]/ CASBn	MA01 [0]	MA01]0]	MA01 [0]	MA01 [0]	MA01 [0]	MA01 [0]	r2,3,6,7 CASBn
MA23 [0[	MA23 [0]	MA23 [0]	MA23 [0]	MA23 [0[	MA23 [0]	MA23 [0]	N.C.

PIN DESCRIPTION

AT-BUS INTERFACE

This section describes the AT-Bus interface signals of the OTI-087 when implemented in an add-on card configuration either on an adapter card or on the motherboard. For information on the system bus interface for local bus implementations, see the next section.

Pin Name	Pin #	Pin Type	Description
SD[15:8]	46:42, 40:38	I/O	SYSTEM DATA BUS 15:8.
SD[7:0]	85:81, 77:75	I/O	SYSTEM DATA BUS 7:0.
SA[16:0]	67:62, 60:50	I	LATCHED SYSTEM ADDRESS BITS 16:0. For add-on card configuration, these are the latched system address bits 16:0.
LA[23:17]	74:68	I	UNLATCHED SYSTEM ADDRESS BITS 23:17. For add-on configuration, these are the unlatched system address bits 23-17. These bits are decoded to generate M16n. Address bits 19:17 are latched by ALE to generate SA[19:17].
M16n	78	I/O	16-BIT MEMORY. This signal is an active low, open drain output signal used to indicate to the system that the present cycle is a 16-bit data transfer to video memory. The signal is derived from the decoding of LA17 through LA23.
IOCHRDY	79	O	I/O CHANNEL READY. This signal is an active high, open drain output that signals to the processor that it is ready for memory access. This signal is used to add wait states to the AT-bus timing during video memory access.
AEN	86	I	ADDRESS ENABLE. This signal is used by the OTI-087 to qualify the video I/O access from the CPU. When it is active high, the DMA controller has control of the address bus, data bus, and command lines.
RFSHn	87	I	REFRESH. This signal is used by the OTI-087 to qualify the video memory access and the I/O access from the CPU. An active low signal indicates a system memory refresh cycle.
MRDn	88	I	MEMORY READ. This is an active low memory read strobe, asserted during memory read cycles.
MWRn	89	I	MEMORY WRITE. This is an active low memory write strobe, asserted during memory write cycles.

Pin Name	Pin #	Pin Type	Description
CINTn	90	O	CRT INTERRUPT REQUEST. An interrupt request is generated when vertical retrace occurs if it is enabled by bit 5 in the Vertical Retrace End register. It is an active low open collector output.
IO16n	91	O	16-BIT I/O. This active low, open drain output signal is used to indicate to the system that the present data transfer is a 16-bit I/O cycle. It is derived from an address decode.
MASTERn	92	I	MASTERn. This pin indicates that the current cycle is a master cycle when the controller is in add-on configuration. It enables the LA address to pass through during master cycle.
ALE	93	I	ADDRESS LATCH ENABLE. This pin is used to latch a valid address from the microprocessor in add-on configuration.
ROMENL	95	I/O	ROM LOW BYTE ENABLE. This active low signal enables the low byte of BIOS data to the CPU data bus in 16-bit BIOS configuration. In 8-bit BIOS configuration, this pin is not used.
RSET	97	I	RESET. This is an active high system reset signal. This input signal will reset the VGA controller and initialize the configuration register based on the logic level on MD[15:0] pins at power-up reset. In a local bus configuration with Oak Technology's system logic chipsets, this pin is connected to system reset, and is used to determine the processor clock phase.
ENVGA	98	I	VGA ENABLE. In non-local bus configurations, this pin acts as the address select for the controller. The selected address range includes the VGA address space, color palette register address space, video memory space and the VGA BIOS space. The address select condition is enabled by register $3C3_H$ bit 0 and register 102_H bit 0.
ZEROWSn	99	I/O	ZERO WAIT STATE. This pin is used to indicate the current cycle is a zero wait state AT-bus cycle.
BHEn	100	I	BYTE HIGH ENABLE. This active low input indicates that there is valid data on the SD[15:8] bus. This signal and SA[0] together indicate to the OTI-087 whether an 8-bit or 16-bit cycle is being executed by the system.
IORn	101	I	I/O READ. This is an active low I/O read strobe, asserted during I/O read cycles.
IOWn	102	I	I/O WRITE. This is an active low I/O write strobe, asserted during I/O write cycles.

LOCAL BUS INTERFACE

Pin Name	Pin #	Pin Type	Description
CA[23:17]	74:68	I	CPU ADDRESS BITS 23:17.
CA[16:0]	67:62, 60:50	I	CPU ADDRESS BITS 16:0. For 80386SX local bus, these pins can be connected directly to the CPU address bus. For 80386/80486 local bus configurations, CA[16:2] sbould be connected to CPU address bits [16:2] and CA[1:0] should be connected to SA[1:0] of the AT bus.
ADSn	93	I	ADDRESS STATUS. This input from the CPU indicates when a valid address is on the bus.
PROCLK	95	I/O	PROCESSOR CLOCK. The processor clock input samples the CPU status and address. This is a 1X clock for 486 CPUs and a 2X clock for 386 CPUs.
WRn	98	I	WRITE/READ. This input from the CPU distinguishes between write and read cycles.
DCn	99	I/O	DATA/CONTROL. This input from the CPU distinguishes between data cycles and control cycles.
HLDA	92	I	HOLD ACKNOWLEDGE. This CPU input indicates a DMA or Master cycle.
ATOEHn	47	O	AT-BUS HIGH BYTE DATA ENABLE. This is an active low output enable signal for AT-bus bigh byte data. This pin is used with 80386DX/80486 local bus configurations. See 80386DX/80486 local bus diagrams for details.
ATOELn	10	I/O	AT BUS LOW BYTE DATA ENABLE. This is an active low output enable signal for AT-bus low byte data. This pin is used with 80386DX/80486 local bus configuration. See 80386DX/80486 local bus diagrams for details.
DIR	11	I/O	DATA DIRECTION CONTROL. This signal controls tbe direction of the data buffer between either the AT-bus or the CPU local bus and the VGA bus. A logical high directs data into the VGA and a logical low provides data output to the AT or CPU bus. This pin is used with 80386DX/80486 local bus configurations. See 80386DX/80486 local bus diagrams for details.
SDLOEn	12	I/O	SYSTEM DATA LOW OUTPUT ENABLE. This active low signal is used to enable the low word data buffer from the CPU bus to the VGA bus. This signal is used with 80386DX/80486 local bus configurations. See 80386DX/ 80486 local bus diagrams for details.
SDHOEn	13	I/O	SYSTEM DATA HIGH OUTPUT ENABLE. This active low signal is used to enable the high word data buffer from the CPU bus to the VGA bus. This signal is used with 80486 local bus configuration. See the 80486 local bus diagram for details.

Pin Name	Pin #	Pin Type	Description
CPUA0	14	I/O	CPU ADDRESS BIT 0. This is the translated CPU address bit 0 that is generated from the 4 byte enahles of the CPU by implementing an external PAL. This signal is used with 80386DX/80486 local hus configurations. See 80386DX/80486 local bus diagrams for details.
CPUA1	15	I/O	CPU ADDRESS BIT 1. This is the translated CPU address bit 1 that is generated from the 4 byte enables of the CPU by implementing an external PAL. This signal is used with 80386DX/80486 local hus configurations. See 80386DX/80486 local hus diagrams for details.
CPUBHEn	16	I/O	CPU BYTE HIGH ENABLE. This active low input is the translated hyte high enahle generated from the 4 hyte enahles of the CPU hy the external PAL. This signal is used with 80386DX/80486 local hus configurations. See 80386DX/80486 local bus diagrams for details.
CPURESET	17	I/O	CPU RESET. This is the reset signal synchronized with the CPU clock. It is used by the VGA controller to determine the correct sampling phase.
GA20	19	I	GATE A20. This signal is used only with local bus configuration.
SRDYI	20	I	SYSTEM READY INPUT. This input from the system chipset indicates the termination of a cycle. This signal is used with 80386DX/80486 local hus configurations. See 80386DX/80486 local bus diagrams for details.
LBSELn	23	O	LOCAL BUS SELECT. This active low signal indicates to 80386DX or 80486 system controller chipsets that the current cycle is a video local hus cycle and that the chipset should not respond to the CPU. This signal also indicates to the CPU that the current cycle is a 16-hit cycle. This signal is used only with 80386DX/80486 local hus configurations. See 80386DX/80486 local hus diagrams for details.
SRDY	78	I/O	SYSTEM READY. This tri-state, active low output indicates the termination of a CPU bus cycle. For chipsets with separate SRDYI and SRDYO, this signal is sampled hy the system controller chipset to indicate the actual termination of the bus cycle. This signal is driven high for one-half of the PROCLK hefore heing tri-stated at the end of a cycle.

CLOCK INTERFACE

Pin Name	Pin #	Pin Type	Description
VCLK	106	I	VIDEO CLOCK. This is the master input pixel clock.
MCLK	107	I	MEMORY CLOCK. This is the input clock used for memory timing.
CSEL[0]	105	O	CLOCK SELECT LINE 0. Clock select lines are used to select the appropriate pixel clock frequency. This pin can be programmed through register $3DF_H$ index 6 or register $3C2_H$.

Pin Name	Pin #	Pin Type	Description
CSEL[1]	104	O	CLOCK SELECT LINE 1. Clock select lines are used to select the appropriate pixel clock frequency. This pin can be programmed through register $3DF_H$ index 6 or register $3C2_H$.
CSEL[2]	103	I/O	CLOCK SELECT LINE 2. Clock select lines are used to select the appropriate pixel clock frequency. This pin can be programmed through register $3DF_H$ index 6.
CSEL[3]	18	O	CLOCK SELECT LINE 3. Clock select lines are used to select the appropriate pixel clock frequency. This pin can be programmed through register $3DF_H$ index 6.

CRT AND COLOR PALETTE INTERFACE

Pin Name	Pin #	Pin Type	Description
P[7:0]	33:30, 28:25	O	PIXEL DATA. This is the 8-bit pixel data bus (bits 7-0). This output bus interfaces to an external palette chip for color mapping during CRT display.
VSYNC	34	O	VERTICAL SYNC. This signal provides the vertical synchronization pulses for the display monitor. The polarity of the pulse is determined by bit 7 of the Miscellaneous Output Register.
HSYNC	35	O	HORIZONTAL SYNC. This signal provides the horizontal synchronization pulses for the display monitor. The polarity of the pulse is determined by bit 6 of the Miscellaneous Output Register.
BLANKn	36	O	BLANK. This active low output signal provides blanking to the color palette to blank the pixel data for the display monitor.
PCLK	37	O	PIXEL CLOCK. The pixel clock output latches the pixel data P7-P0 to the color palette. The clock rate is selected by the clock select pins for the current video mode.
DACRDn	48	O	COLOR PALETTE READ. This active low I/O read signal is generated for reading external color palette registers.
DACWRn	49	O	COLOR PALETTE WRITE. This active low I/O write signal is generated for writing to external color palette registers.
BD[7:0]	17:10	I/O	AUXILIARY DATA BUS 7:0. In add-on card mode, this bus is the high byte data (bits 7-0) of the VGA BIOS in 16-bit BIOS configuration or the single byte data in 8-bit BIOS configuration. In 80386DX/80486 local bus configurations, BD[7:0] are used as miscellaneous signals to control the data routing to and from the VGA bus, the AT-bus and the CPU local bus.

Pin Name	Pin #	Pin Type	Description
EPCLK	19	I	ENABLE PCLK. This active high input is used to enable the PCLK output.
EPDATA	20	I	ENABLE PDATA. This active high input is used to enable the PDATA.
MXPCLK	23	O	MUX CLOCK. For 24-bit color mode support with a color palette that requires a 24-bit bus, this clock signal is used as the PCLK for latching PDATA to a bank of external data latches.
SWSENSE	24	I	SWITCH SENSE. This input signal is used to auto-detect the monitor type.

VIDEO MEMORY INTERFACE

Pin Name	Pin #	Pin Type	Description
MA01[8:1]	134:131, 129:126		MEMORY ADDRESS MAPS 0, 1. Memory address for maps 0,1 bits 8:1 for 256KxXX and 512Kx8 DRAMs, bits 7:0 for 64Kx16 DRAMs.
MA23[8:1]	115:108		MEMORY ADDRESS MAPS 2, 3. Memory address for maps 2,3 bits 8:1 for 256KxXX and 512Kx8 DRAMs, bits 7:0 for 64Kx16 DRAMs.
RASLn	120	O	ROW ADDRESS STROBE LOW. This active low output signal connects to the first 1 MByte of 256KxXX DRAMs, the first 512Kbytes of 64Kx16 DRAM's, and all banks of 512Kx8 DRAMs.
RASHn/ MA9	125	O	ROW ADDRESS STROBE HIGH. This active low output signal connects to the second 1 MByte of 256KxXX DRAMs or the second 512Kbytes of 64Kx16 DRAMs. For 512Kx8 DRAMs, this pin is memory address bit 9, and should be connected to all maps and all banks of 512Kx8 DRAMs.
CASAn/ WEn	123	O	COLUMN ADDRESS STROBE/WRITE ENABLE. This active low output signal connects to all video memory maps and to all banks of 256KxXX. CASAn connects to all video maps of 512Kx8, but only to maps 0, 1 of all banks of 64Kx16 DRAMs.
WEAn/ CAS0n	118	O	WRITE ENABLE A/COLUMN ADDRESS STROBE 0. This active low write enable signal connects to memory maps 0 and 1 in 16-bit MD configurations (4 - 256Kx4, 2 - 512Kx8), and is the write enable/column address strobe for memory map 0 in 32-bit MD configuration.
WEBn/ CAS1	119	O	WRITE ENABLE B/COLUMN ADDRESS STROBE 1. This active low write enable signal connects to memory maps 2 and 3 in 16-bit MD configurations (4 - 256Kx4, 2 - 512Kx8), and is the write enable/column address strobe for memory map 2 in 32-bit MD configuration.
WECn/ CAS2n	116	O	WRITE ENABLE C/COLUMN ADDRESS STROBE 2. This active low write enable/column address strobe signal connects to memory map 1 in 32-bit MD configuration.

Pin Name	Pin #	Pin Type	Description
WEDn/ CAS3n	117	O	WRITE ENABLE D/COLUMN ADDRESS STROBE 3. This active low write enable/column address strobe signal connects to memory map 3 in 32-bit MD configuration.
MA01[0]/ CASBn	124	O	MAP 0,1 MEMORY ADDRESS BIT 0. Memory address bit 0 for maps 0,1 in 256KxXX and 512Kx8 DRAM configurations. This signal is CASBn for maps 1, 3 in 64Kx16 DRAM configurations.
MA23[0]	122	O	MAP 2,3 MEMORY ADDRESS BIT 0. This signal is memory address bit 0 for maps 2,3 in 256KxXX and 512Kx8 DRAM configuration.
MD[31:0]	9:2, 160:153, 152:145, 143:142, 140:135	I/O	MEMORY DATA. This is the memory data bus, bits 31-0. MD[15:0] are also used for the configuration register during hardware reset. MD[7:0] correspond to bits 7:0 of Configuration Register 1 and MD[15:8] correspond to bits 7:0 of Configuration Register 2. See Memory Mapping table and block diagrams for further details.

EEPROM INTERFACE

Pin Name	Pin #	Pin Type	Description
EEPCSn	47	O	EEPROM CHIP SELECT. This signal is used to enable the serial EEPROM for read and write operations.
EEPSK	103	O	EEPROM SHIFT CLOCK. This clock can be toggled through register $3DF_H$ index 18_H.
EEPWD	104	O	EEPROM WRITE DATA. Data can be written to the EEPROM through the data bit in the register $3DF_H$ index 18_H.
EEPRD	105	I/O	EEPROM READ DATA. Data can be read from the EEPROM through the data read bit in the register $3DF_H$ index 18_H.

POWER & GROUND

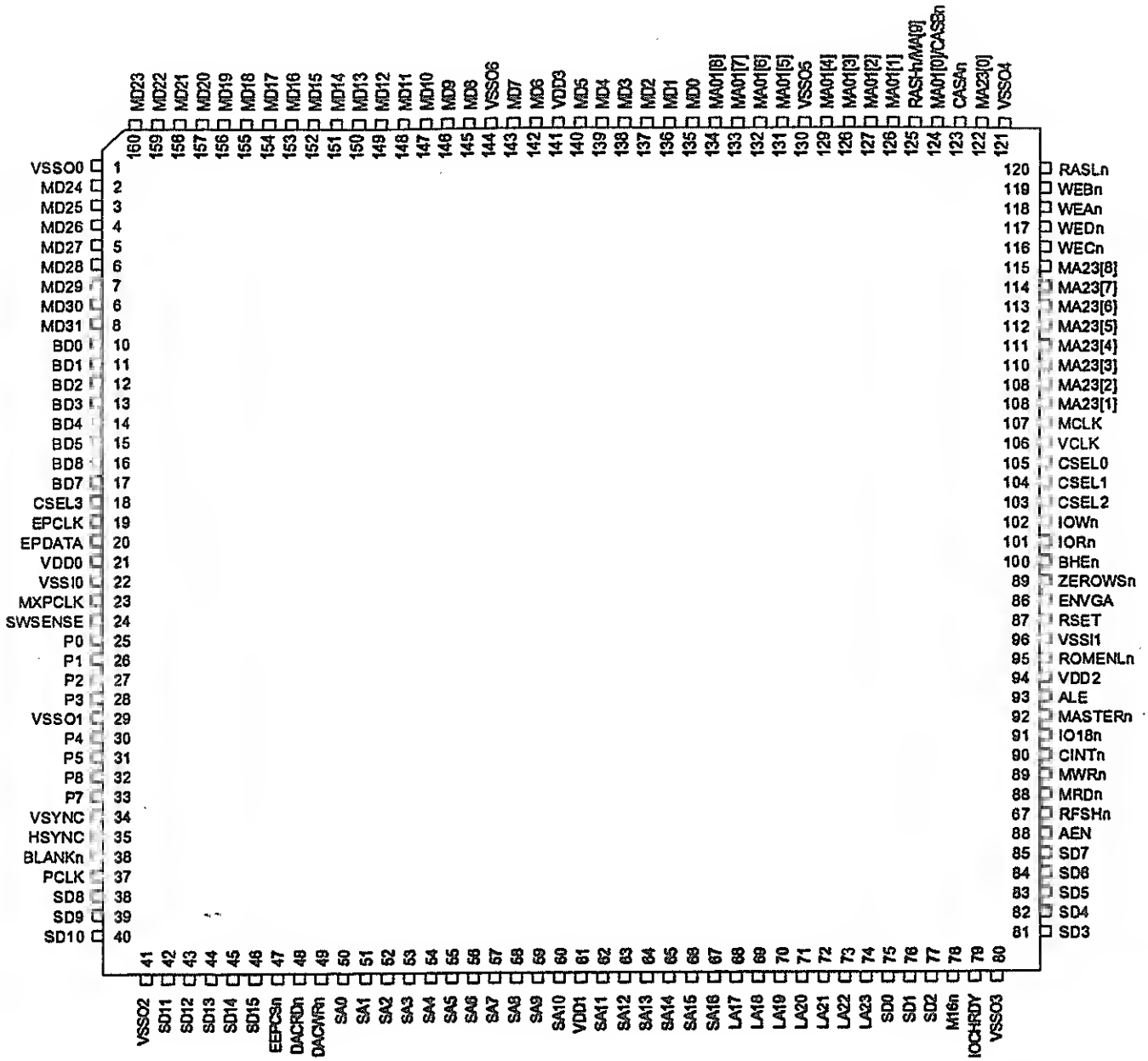
Pin Name	Pin #	Pin Type	Description
VSSO0, VSSO1,VSSO2, VSSO3,VSSO4, VSSO5,VSSO6	1, 29,41, 80,121, 130,144		EXTERNAL GROUND.
VSSI0, VSSI1	22, 96		INTERNAL GROUND.
VDD0, VDD1,VDD2, VDD3.	21, 61,94, 141		EXTERNAL & INTERNAL POWER.

Pin Out Cross Reference for OTI-087 in Different Configurations

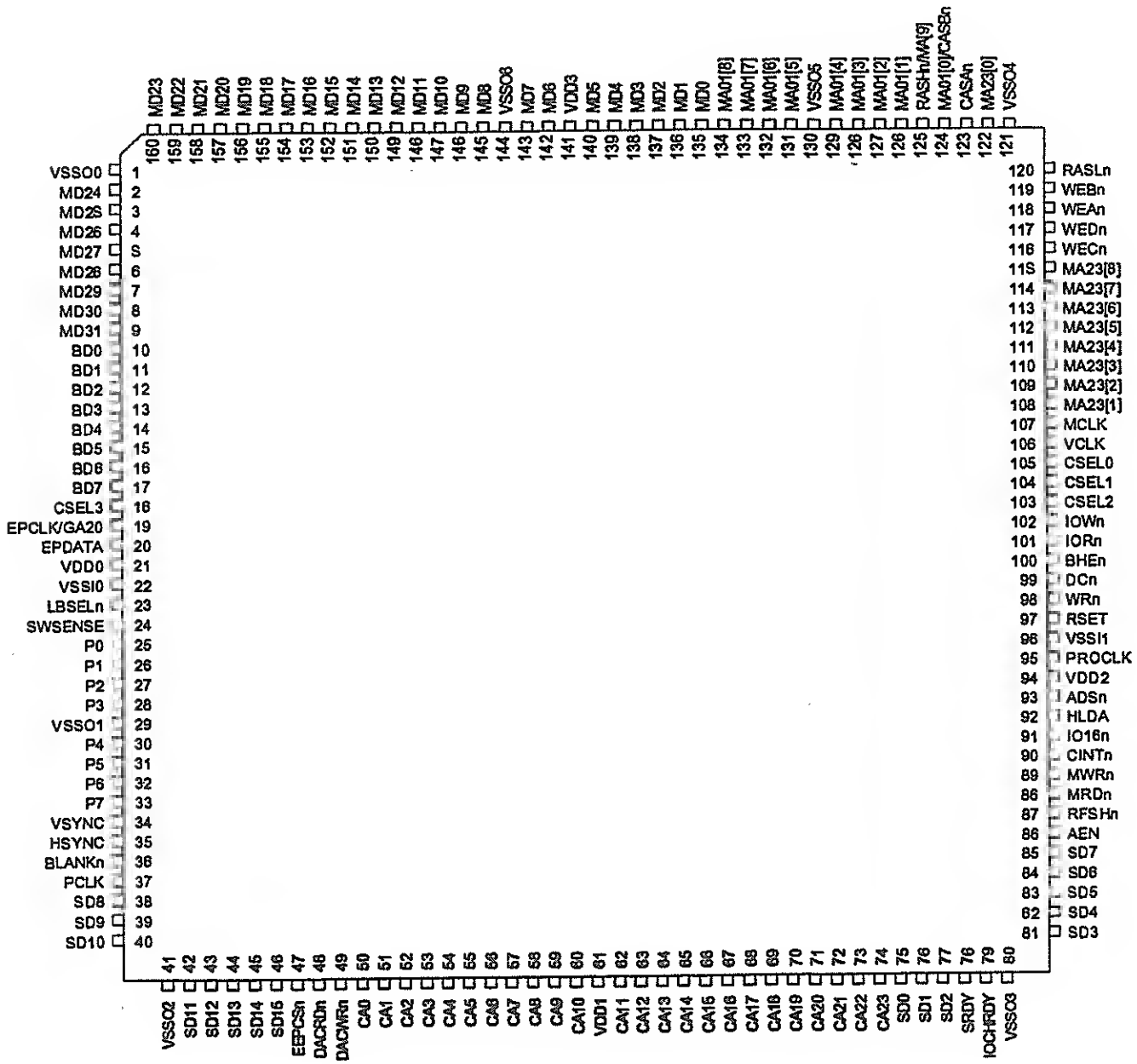
Pin #	OTI-087 (ISA Add-on)	OTI-087 (Oak LB)	OTI-087 (LB 386/486)
1	VSSO0	VSSO0	V55O0
9:2	MD[31:24]	MD[31:24]	MD[31:24]
10	BD[0]	BD[0]	ATOELn
11	BD[1]	BD[1]	DIR
12	BD[2]	BD[2]	SDLOEn
13	BD[3]	BD[3]	SDHOEn
14	BD[4]	BD[4]	CPUA0
15	BD[5]	BD[5]	CPUA1
16	BD[6]	BD[6]	CPUBHEn
17	BD[7]	BD[7]	EEPCSn
18	CSEL[3]	CSEL[3]	CSEL[3]
19	EPCLK	EPCLK/GA20	EPCLK
20	EPDATA	EPDATA	SRDYI
21	VDD0	VDD0	VDD0
22	VS5I0	VS5I0	VSSI0
23	MXPCLK	LB5ELn	LB5ELn
24	5W5ENSE	5W5ENSE	SWSENSE
33:30,28:2S	P[7:0]	P[7:0]	P[7:0]
29	V5SO1	VSSO1	VS5O1
34	VSYNC	VSYNC	V5YNC
35	HSYNC	HSYNC	HSYNC
36	BLANKn	BLANKn	BLANKn
37	PCLK	PCLK	PCLK
46:42,40:38	SD[15:8]	5D[15:8]	5D[15:8]
41	VSSO2	VSSO2	VSSO2
47	EEPCSn	EEPCSn	ATOEHn
48	DACRDn	DACRDn	DACRDn
49	DACWRn	DACWRn	DACWRn
S1:S0	SA[1:0]	CA[1:0]	SA[1:0]
67:62,60:S2	SA[16:2]	CA[16:2]	CA[16:2]
74:68	LA[23:17]	CA[23:17]	CA[23:17]
61	VDD1	VDD1	VDD1
8S:81,77:75	SD[7:0]	SD[7:0]	SD[7:0]
78	M16n	SRDY	SRDY
79	IOCHRDY	IOCHRDY	IOCHRDY
80	VSSO3	VSSO3	VSSO3
86	AEN	AEN	AEN
87	RFSHn	RFSHn	RFSHn
88	MRDn	MRDn	MRDn
89	MWRn	MWRn	MWRn
90	CINTn	CINTn	CINTn
91	IO16n	IO16n	IO16n
92	MASTERn	HLDA	HLDA

Pin #	OTI-087 (ISA Add-on)	OTI-087 (Oak LB)	OTI-087 (LB 386/486)
93	ALE	ADSn	ADSn
94	VDD2	VDD2	VDD2
95	ROMENLn	PROCLK	PROCLK
96	VSSI1	VSSI1	VSSI1
97	RSET	RSET	RSET
98	ENVGA	WRn	WRn
99	ZEROWSn	DCn	EPDATA
100	BHEn	BHEn	BHEn
101	IORn	IORn	IORn
102	IOWn	IOWn	IOWn
103	CSEL[2]	CSEL[2]	CSEL[2]
104	CSEL[1]	CSEL[1]	CSEL[1]
105	CSEL[0]	CSEL[0]	CSEL[0]
106	VCLK	VCLK	VCLK
107	MCLK	MCLK	MCLK
115:108,122	MA23[8:0]	MA23[8:0]	MA23[8:0]
116	WECn	WECn	WECn
117	WEDn	WEDn	WEDn
118	WEAn	WEAn	WEAn
119	WEBn	WEBn	WEBn
120	RASLn	RASLn	RASLn
121	VSSO4	VSSO4	VSSO4
123	CASAn	CASAn	CASAn
134:131, 129:126	MA01[8:1]	MA01[8:1]	MA01[8:1]
124	MA01[0]/ CASBn	MA01[0]/ CASBn	MA01[0]/ CASBn
125	RASHn/MA9	RASHn/MA9	RASHn/MA9
130	VSSO5	VSSO5	VSSO5
152:145,143, 142,140:135	MD[15:0]	MD[15:0]	MD[15:0]
141	VDD3	VDD3	VDD3
144	VSSO6	VSSO6	VSSO6
160:153	MD[23:16]	MD[23:16]	MD[23:16]

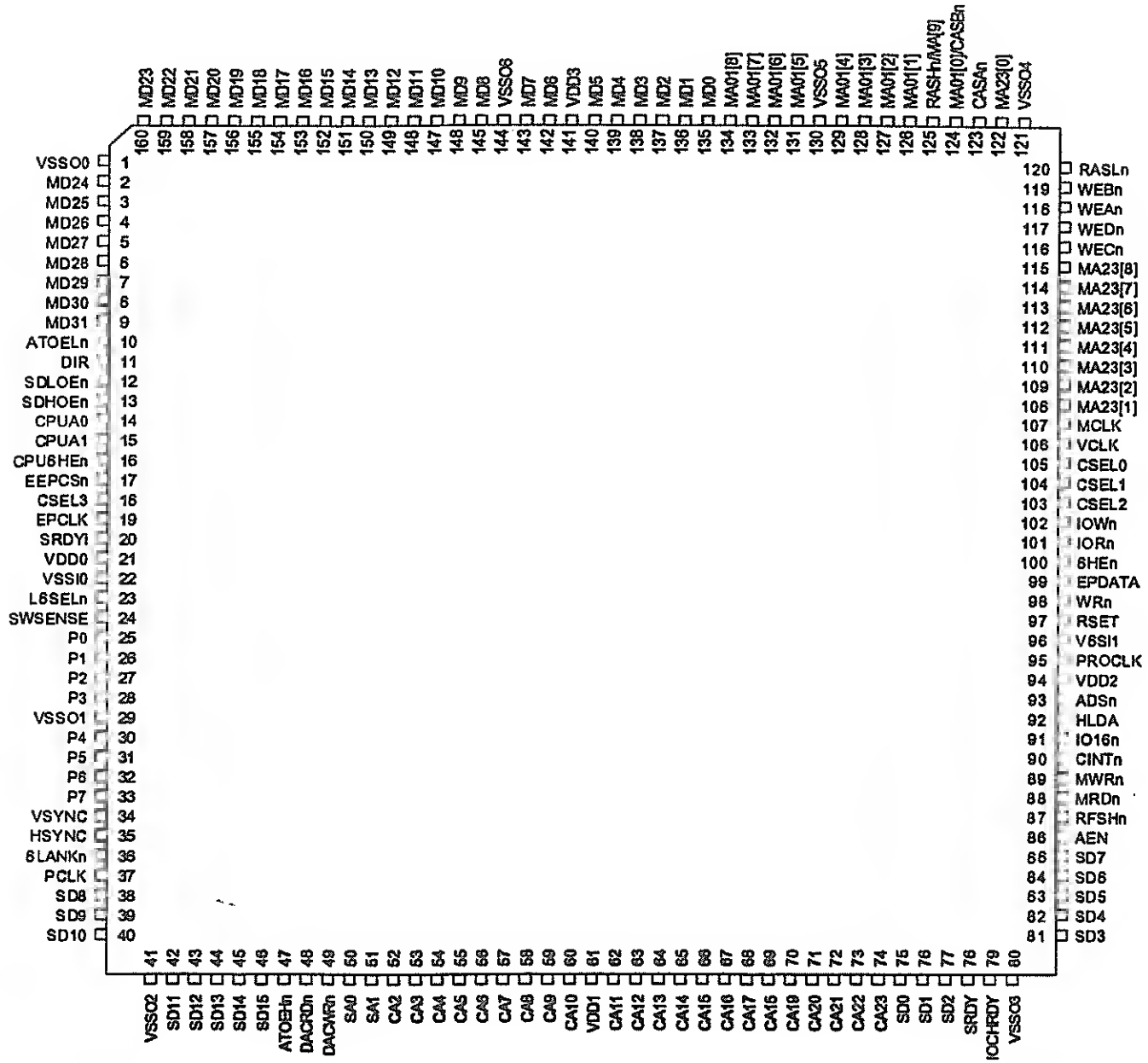
OTI-087 ISA Add-on Pin Diagram



OTI-087 Oak LB Pin Diagram



OTI-087 LB 386/486 Pin Diagram



OTI-087 Register Definitions

Refer to OTI-067 databook or IBM technical reference for VGA register definition. All registers are in hexadecimal format. Local bus related registers follow:

Local Bus Related Registers

1F Video memory range control register Index = 5 W

Bit	Description
0	VMS0: En/Dis video memory A0000 - AFFFF (64K).
1	VMS1: En/Dis video memory B0000 - B0FFF (4K).
2	VMS2: En/Dis video memory B1000 - B3FFF (16K).
3	VMS3: En/Dis video memory B4000 - B7FFF (16K).
4	VMS4: En/Dis video memory B8000 - BBFFF (16K).
5	VMS5: En/Dis video memory BC000 - BFFFF (16K).
7-6	Reserved.

Default : 1F

Adapter Card/Motherboard Configuration

There are two sets of registers that control the IBM VGA products. One register set controls access to the on-board, system VGA and the other register set controls access to the add-on VGA. These registers are used to enable or disable the appropriate VGA interface. The OTI-087 chip contains both add-on and on-board registers. The registers that control on-board operation also reside in the system chipset or on the motherboard. The addresses for both register sets are:

Add-on VGA mode	46E8	control (in OTI-087)
	0102	enable/disable (in OTI-087)
On-board VGA mode	03C3	enable/disable (in OTI-087)
	0094	control (in OTI-087 and system chip)
	0102	enable/disable (in OTI-087)

Add-On Mode Configuration

In order for the OTI-087 to properly function in the add-on mode, the following initialization sequence is recommended. This example assumes no BIOS ROM paging.

46E8	<=	10	Enable access to location 0102 in VGA chip.
0102	<=	01	Enable VGA chip.
46E8	<=	08	Activate read/write access to VGA interface.

Once in this mode, 46E8 bit 3 may be cleared to disallow access or may be set to permit access to the VGA interface registers. However, if 102 in the VGA chip is not loaded with a 1, 46E8 bit 3 has no effect and the VGA interface registers will not respond to read or write commands.

Registers 46E8 and 102 are described below.

46E8 **W**

This is a write-only register. This register serves as the Power on Setup (POS) equivalent on Micro Cbannel Architecture (MCA) machines.

Bit	Description
2-0	Reserved.
3	VGA, Color Palette, and Video RAM access control.

Bit 3	Description
0	Disable read/write access to VGA/Color Palette/Video RAM.
1	Enable read/write access to VGA/Color Palette/Video RAM (normal operational mode).

4 This bit sets the current state of the OTI-087 in add-on mode.

Bit 4	Description
0	Add-on card is in the ACTIVE state (this is the normal mode of operation for tbe add-on mode).
1	Add-on card is in the SETUP state. This permits a software utility to enable or disable access to tbe OTI-087 chip.

7-5 Reserved.

102 **R/W**

Bit	Description
0	VGA, Color Palette, and Video RAM access control.

Bit 0	Description
0	Disable read/write access to VGA/Color Palette/Video RAM.
1	Enable read/write access to VGA/Color Palette/Video RAM.

7-1 Reserved.

On-Board Mode Configuration

When the OTI-087 is configured to operate on a system motberboard, the ENVGA pin or register 3C3 in conjunction with registers 94/102 controls access to the OTI-087. To access the OTI-087 chip, ENVGA should be asserted or register 3C3 bit 0 set to 1. Register 102 bit 0 should also be set to 1. To access register 102 in on-board configuration, OTI-087's register 94 bit 5 should be written with a 0. The definition of register 94 inside OTI-087 is given below.

94 **W**

This is a write only register.

Bit	Description
4-0	Reserved.
5	VGA, Color Palette, and Video RAM access control.

Bit 5	Description
0	Disable read/write access to VGA/Color Palette/Video RAM. Enable write to register 102.
1	Enable read/write access to VGA/Color Palette/Video RAM. Disable write to register 102.

7-6 Reserved.

3DF Oak Test Register — Index = 3 — R/W

Bit	Description
2-0	Test mode - These bits define the test modes of the controller.

Bits 2-0	Test mode
000	Test CRTC.
001	Reserved.
010	Test waveform RAM.
011	Reserved.
100	Reserved.
101	Scan Test Attribute Controller. This bit forces the font data and attribute data to be replaced by the system data bus 15:8 and 7:0 respectively in text mode. In graphic mode, this bit replaces the APA data with system data bus 15:8.
110	Reserved.
111	Reserved.

Bit	Description
3	Reserved.
4	Cache Flush

Bit 4	Description
0	Normal operation.
1	Flush the write cache immediately after a write command.

Bit	Description
5	VSYNC Test. This bit will cause the V-sync to toggle when it is changed from 1 to 0 or from 0 to 1.
6	I/O write test bit.

Bit 6	Description
0	Normal operation.
1	I/O test mode - In this mode, an I/O write command is not clocked by MCLK. Bit 6 must be 0 during normal operation.

Bit	Description
7	Enable test mode.

Bit 7	Description
0	Normal operation.
1	Enable global test modes. Bit 7 must be 0 during normal operation.

Default: 0

3DF Local Bus Control Register — Index = 4 — R/W

Bit	Description
0	First write wait state.

Bit 0	Description
0	No additional wait state for the first write cycle (the first write cycle is a memory write cycle when the write cache is empty).
1	One wait state is inserted into the first write cycle. This bit should be turned on when the OTI-087 is operated with 20 MHz 80286 CPU, or 40 MHz or higher frequency 80386 and 80486 CPU.

1 Write hit wait state.

Bit 1	Description
0	No additional wait state for write hit cycle (a write hit cycle is a write cycle which shares the same cache page address with the previous write).
1	One wait state is inserted into each local bus write hit cycle. This bit should be turned on when the controller is operated with 40 MHz or higher frequency 80386 and 80486 CPU's.

2 Read hit wait state.

Bit 2	Description
0	No additional wait state for read hit cycle (a read hit cycle is a read cycle in which the content of the read already exists in the read cache).
1	One wait state is inserted into each local bus read hit cycle. This bit should be turned on when the controller is operated with 40 MHz or higher frequency 80386 and 80486 CPU's.

3 80486 Minimum wait state.

Bit 3	Description
0	Zero-wait-state 80486 local bus.
1	Minimum 1-wait-state 80486 local bus. This bit has no effect on configurations other than 80486 local bus.

4 Turbo local bus interface.

Bit 4	Description
0	Normal local bus operation (OTI-087 Rev A and OTI-087 Rev B)
1	Enable this bit for faster local bus performance.

7-4 Reserved.

Default: F

3DF Video Memory Mapping Register Index = 5 R/W

Bit Description

0 Enable Oak address mapping.

Bit 0	Description
0	VGA memory mapping at A0000 and B8000 as dictated by Graphic register 6.
1	Oak memory mapping as dictated by bit 2 and 3 of this register.

1 DMA access disable.

Bit 1	Description
0	Normal operation.
1	Disable DMA access to video memory. This bit is used when the OTI-087 linear address range is to be higher than 16 Mbytes.

3-2 Memory address aperture select. These bits define the memory address aperture for which the OTI-087 will respond. These bits have no effect if bit 0 = 0.

Bits 3,2	Memory address aperture
00	x00000-x3FFFF: 256K aperture.
01	x00000-x7FFFF: 512K aperture.
10	x00000-xFFFFF: 1M aperture.
11	x00000-1FFFFF: 2M aperture.

7-4 These bits define the starting address range for the OTI-087.

Bits 7-4	Start address
0000	000000 - only VGA memory mapping (A0000-BFFFF).
0001	100000
....	..:....
1111	F00000

For 2 Mbyte aperture, the starting address has to be multiple of 2 Mbyte.
Default: 0

3DF Clock Select Register Index = 6 R/W

Bit Description

3-0 Video Clock Select. The state of these 4 bits are reflected in the pins CSEL[3:0]. Bits 1-0 of this register are the images of bits 3-2 of register 3C2. Bit 2 of this register is the image of bit 5 of extended register D. See frequency table for more details. This frequency table reflects OTI-068 only. Future Oak clock chips may have different frequencies.

Frequency Table for OTI-068

CSEL3	CSEL2	CSEL1	CSEL0	CLOCK (MHz)
0	0	0	0	25.2
0	0	0	1	28.3
0	0	1	0	65.0
0	0	1	1	44.9
0	1	0	0	28.3
0	1	0	1	36.0
0	1	1	0	40.0
0	1	1	1	36.0
1	0	0	0	25.2
1	0	0	1	28.3
1	0	1	0	78.0
1	0	1	1	65.0
1	1	0	0	63.0
1	1	0	1	72.0
1	1	1	0	40.0
1	1	1	1	50.0

7-4 Reserved.

Software reset must be executed each time this register is updated.

Default: 0

3DF Configuration Register 1 Index = 7 R

Bit	Description
0	BIOS path width selection.

Bit 0	Description
0	8-bit BIOS (1 ROM)
1	16-bit BIOS (2 ROM's)

2-1 Bus Modes. These bits define the bus configuration of the controller. For different types of local bus configurations, see Configuration Register 2, bits 1 and 0.

Bits 2,1	Bus Modes
00	Local bus Motherboard. When this mode is selected, the OTI-087 must be enabled through port 94/102 and 3C3. This mode also disables ROM decoding at C0000.
01	Local bus Add-on. When this mode is selected, the OTI-087 must be enabled through port 46E8/102 and enables ROM decoding at C0000.
10	Motherboard, AT-bus configuration. In this configuration, the OTI-087 is enabled through 94/102 and either 3C3 or ENVGA and does not respond to C0000.
11	Add-on card, AT-bus configuration. In this configuration, the OTI-087 is enabled through 46E8/102 and responds to C0000.

4-3 DRAM type. These bits define the type of DRAM used.

Bits 4,3	DRAM Type
00	64Kx16
01	Reserved.
10	256KxXX
11	512Kx8.

5 Configuration for pin 92 when in local bus configuration (bit 2 of this register = 0).

Bit 5	Description
0	pin 92=MASTERn
1	pin 92=HLDA

6 I/O write sampling clock speed. IOWn from the AT-bus is internally sampled with MCLK, thus it is important to indicate to the I/O controller the MCLK speed.

Bit 6	Description
0	MCLK >= 44 MHz
1	MCLK < 44 MHz.

7 CPU Clock select.

Bit 7	Description
0	Normal system clock; 2X clock for 386, 1X clock for 486.
1	VL-Bus CPU clock; 1X clock for 386.

Bit 2 and bit 7 of tbis register in combination with bits 1,0 of Configuration Register 2 are used to enable tbe EEPROM function for capable 386/486 local bus configurations.

Index=7	Index=8		
Bit 7 2	Bit 1 0	Pin 17	Description
x 0	0 0	BD[7]	Oak Local Bus
0 0	x x	CPURESET	386/486 Local Bus
0 1	x x	BD[7]	AT-Bus
1 0	x x	EEPCSn	386/486 Local Bus

The contents of this register are loaded from MD[7:0] during hardware reset.

3DF Configuration Register 2 Index = 8 R

Bit	Description
1-0	Local bus interface select bits - These bits define local bus type. These bits only have effect when bits 2 and 1 of Configuration Register 1 are 00.

Bits 1,0	Bus Type
00	Oak local bus.
01	80386 local bus interface.
10	80486 local bus interface.
11	Reserved.

3-2 Color Palette interface select bits.

Bits 3,2	Color Palette Type
00	Type 0: BT476, SC11487, IMSG174 or equivalent.
01	Type 1: MU9C1715 or equivalent.
10	Type 2: BT484 or equivalent.
11	Reserved.

For Type 0, PCLK is passed through. For Types 1 and 2, PCLK is divided by two when in Hi-color mode and divided by three when in true color mode. Also, for Types 1 and 2, MUXCLK is generated to latch pixel data. For Type 2, BLANKn is delayed by 1 divided PCLK.

5-4 Reserved.

6 Enable Feature Connector for select local bus configurations. Bits 0, 1, and 6 of this register determine the function of pins 19 and 20. Bit 6 can only be enabled when GA20 and SRDYi are not needed.

Bits 6, 1, 0	Pin 19	Pin 20	Pin 99
0 0 0	GA20	N.C.	DCn
0 0 1	GA20	SRDYi	DCn
0 1 0	GA20	SRDYi	DCn
0 1 1	-	-	-
1 0 0	EPCLK	EPDATA	DCn
1 0 1	EPCLK	SRDYi	EPDATA
1 1 0	EPCLK	SRDYi	EPDATA
1 1 1	-	-	-

7 DRAM support bit. This bit determines whether pins 116-119 and pin 123 is a write enable or CAS pin for different DRAM types.

The contents of this register are loaded from MD[15:8] during hardware reset.

Bit	Pin 123	Pin 118	Pin 119	Pin 116	Pin 117
0	CASAn	WEAn	WEBn	WECn	WEDn
1	WEn	CASAn	CASBn	CASCn	CASDn

3DF Scratch Registers Index = 9, A, B R/W

Bit	Description
7-0	8 scratch bits.

These scratch pads are defined and reserved for internal use. Application software and device drivers should not use them.

3DF CRT Control Register **Index = C**

Bit	Description
7-0	Not used.

3DF Oak Miscellaneous Register **Index = D** **R/W**

Bit	Description
2-0	FIFO depth control. A minimum memory FIFO depth is filled with display data before CPU read/write request is allowed to process. These bits are the image of index register 20 bits 2-0.
4-3	Extended graphics mode selection. These two bits are the image of extended register 21 bits 3-2.

Bits 4,3	Mode Selection
00	VGA modes or Oak planar modes.
01	Oak packed pixel modes. Used for 256, 32K, 64K and 16M color modes.
10	Reserved.
11	Reserved.

5	Clock select bit 2 (CSEL2). Used with bits 2 and 3 of Miscellaneous register in the general registers area to select different clock frequencies.. Up to eight different clock inputs can be selected. This bit is the image of extended register 6 bit 2. Refer to extended register 6 for clock table.
7-6	Reserved.

This register is for compatibility purposes only. New software development should use extended registers 6, 20 & 21. Software reset must be executed each time this register is updated.
Default: 0

3DF Backward Compatibility Register **Index = E**

Bit	Description
7-0	Not used.

3DF NMI Data Cache Register **Index = F**

Bit	Description
7-0	Not used.

3DF Dip Switch Register **Index = 10** **R**

Bit	Description
7-0	Dip switch status register. The contents of this register are loaded from SD[7:0] during hardware reset.

3DF Segment Register **Index = 11** **R/W**

Bit	Description
3-0	Read segment for CPU memory read.
7-4	Write segment for CPU memory write.

These two 4-bit segment registers are used to extend the CPU address for video memory sizes greater tban 256 Kbytes. Bits 3-0 are used to address the video memory read operation. Bits 7-4 are used to address the video memory for write mode operations. Bits 3-0 are the image of index register 23 bits 3-0. Bits 7-4 are the image of index register 24 bits 3-0.

CPUADDR[19:16] = NR11[3:0] for read.
CPUADDR[19:16] = NR11[7:4] for write.

This register is provided for compatibility purposes only. New software development should use registers 23, 24 & 25.
Default: 0

3DF Configuration Register — Index = 12

Bit	Description
7-0	Not used.

3DF Bus Control Register — Index = 13 R/W

Bit	Description
2-0	Reserved.
3	AT-bus Zero-Wait-State enable.
	Bit 3: 0 — Disable zero wait state AT-bus operation.
	Bit 3: 1 — Enable zero wait state AT-bus operation.
4	BIOS ROM bus width selection.
	Bit 4: 0 — Enable 8-bit video BIOS ROM interface.
	Bit 4: 1 — Enable 16-bit video BIOS ROM interface.
5	BIOS ROM address selection.
	Bit 5: 0 — Enable video BIOS ROM access at C0000.
	Bit 5: 1 — Disable video BIOS ROM access at C0000.
6	I/O access bus width selection.
	Bit 6: 0 — 8-bit I/O access.
	Bit 6: 1 — 16-bit I/O access.
7	Video memory bus width selection.
	Bit 7: 0 — 8-bit memory access.
	Bit 7: 1 — 16-bit memory access.

1100 1000

Default: 0

3DF Oak Overflow Register — Index = 14 R/W

Bit	Description
0	Vertical Total Bit 10
1	Vertical Blank Start Bit 10
2	Vertical Retrace Start Bit 10
3	High Order Start Address Bit 8
6-4	Reserved.

7 Enable interlaced display.

Bit 7	Description
0	non-interlaced display.
1	interlaced display.

Default: 0

Note: The High Order Start Address Bit 8 (bit 3 of this register) can also be updated with register index = 17, bit 0.

3DF HSYNC Divided by Two Start Register Index = 15 R/W

Bit	Description
7-0	This 7 bit value indicates when tbe vertical retrace will start in every odd frame during interlaced mode. The unit of this value is in the character position.

3DF Oak Overflow Register 2 Index = 16

Bit	Description
7-0	Not used.

3DF Extended CRTC Register Index = 17 R/W

Bit	Description
2-0	High Order Start Address Bit 10-8.
7-3	Reserved.

Note: The High Order Start Address Bit 8 (bit 0 of this register) can also be updated using register index = 14, bit 3.

3DF EEPROM Control Register Index = 18 R/W

Bit	Description
0	EEPROM Data. This bit is the data line between the serial EEPROM and the VGA controller. When reading this bit, data comes from CSEL[0]. When writing to this bit, data is sent to CSEL[1]. At the board level, CSEL[0] and CSEL[1] are connected to the EEPROM data out and the EEPROM data in pins respectively.
1	EEPROM CS. This bit is used as the chip select control for the EEPROM. It should be set to 1 for tbe VGA controller to access the EEPROM.
2	EEPROM Function Enable. This bit selects the function of the CSEL bus. When this bit is 1, CSEL[2:0] are used to interface with the EEPROM. When this bit is 0, the CSEL[2:0] function as clock select signals.
3	EEPROM Clock(SK). The value of this bit, which acts as the shift clock for the serial EEPROM, is reflected on CSEL[2]. To program the EEPROM, this bit is programmed to toggle between 1 and 0 every 4us.
7-4	Reserved.

Default: 0

3DF Color Palette Range Register **Index = 19** **R/W**

Bit	Description
3-0	Color Palette range. This register, in addition to the IBM VGA Color Palette address range 3C6-3C9, defines the I/O address range for the Color Palette . The Color Palette read and Color Palette write lines of the OTI-087 are activated when the programmable address range 3x0~3xF is accessed. Here x is defined by bits 3-0 of this register. The valid value for this register is 0 to E. A programmed value of F disables the Color Palette range function.
7-4	Reserved.

Default: 4

3DF FIFO Depth Register **Index = 20** **R/W**

Bit	Description
3-0	FIFO depth control. This register defines what minimum level the display FIFO must be filled to for a CPU read/write request to be processed. Bits 2-0 of this register are a mirror image of bits 2-0 of extended register D.
7-4	Reserved.

Default: 1

3DF Mode Select Register **Index = 21** **R/W**

Bit	Description
0	Enable Hi-Color: This bit is used to select the OTI-087 for Hi-Color operation. When this bit is enabled, all horizontal CRT parameters are multiplied by two.
1	Enable True Color: This bit is used to select the OTI-087 for True Color operation. When this bit is enabled, all horizontal CRT parameters are multiplied by three.
3-2	Extended graphics mode selection.

Bits 3,2	Mode Selection
00	VGA modes or Oak planar modes.
01	Oak packed pixel modes. Used for 256, 32K, 64K and 16M color modes.
10	Reserved.
11	Reserved.

Bits 3-2 of his register are a mirror image of bits 4-3 of extended register D.

4-6	Reserved.
7	Select one refresh.

Bit 7	Description
0	Normal operation.
1	When this bit is 1, only one memory refresh cycle will be executed per scan line. This bit overrides bit 6 of CRT register index = 11.

Note: Software reset must be executed each time this register is updated.
Default: 0

3DF Feature Select Register **Index = 22** **R/W**

Bit	Description
0	Enable content addressable for 64-bit graphic latch. When bit 4 is low, and this bit is high, content of the 64-bit graphic latch can be selected from system address to be written out to video memory.
1	Reserved.
2	Enable read cache. This bit enables the read cache in the OTI-087 controller. It should be set to 1 for high performance operation.
3	Enable write cache. This bit enables the write cache in the controller. It should be set to 1 for high performance local bus operations. This bit must not be enabled for AT-bus implementations.
4	Enable 64-bit graphics latch.
5	CPU latch swap. This bit reverses the order of the high and low CPU latch during CPU write operations. This feature is useful when the CPU write address and CPU read address are unaligned.
7-6	Reserved.

Default: 0

3DF Extended Read Segment Register **Index = 23** **R/W**

Bit	Description
4-0	These 5 bits correspond to the CPUADR[20:16] for CPU read operations. They are used to extend the 64K video memory space (A0000-AFFFF). The least significant 4 bits of this register are shared with NR11[3:0]. A write to one of these registers effects the contents of the other register.
7-5	Reserved.

3DF Extended Write Segment Register **Index = 24** **R/W**

Bit	Description
4-0	These 5 bits correspond to the CPUADR[20:16] for CPU write operations. They are used to extend the 64K video memory space (A0000-AFFFF). The most significant 4 bits of this register are shared with NR11[7:4]. A write to one of these registers effects the contents of the other register.
7-5	Reserved.

3DF Extended Common Read Write Register **Index = 25** **R/W**

Bit	Description
4-0	These 5 bits are a write port for both register 23 and 24. A write to this register is equivalent to writing into both index registers 23 and 24. A read to this register is equivalent to reading the extended write segment register.
7-5	Reserved.

3DF Color Expansion Control Register Index = 30 R/W

Bit	Description
0	Enable color expansion mode.

Bit 0	Description
0	Disable color expansion mode
1	Enable color expansion mode. Memory data written to the video memory depends on the contents of the foreground color register, the contents of the background color register and the contents of the color pattern register.

Bit	Description
1	Planar/packed pixel color expansion mode select.

Bit 1	Description
0	Packed pixel color expansion mode.
1	Planar color expansion mode.

Bit	Description
2	Select pattern register for color expansion.

Bit 2	Description
0	The CPU data bus is used to select the foreground and background register.
1	The color pattern register is used to select the foreground and background register.

Bit	Description
3	Pixel mask enable.

Bit 3	Description
0	Disable pixel mask function. In this mode the masking function is compatible with the IBM VGA.
1	Enable pixel mask function. In this mode both the map mask register and the address masking in packed pixel mode is disabled.

Bit	Description
4	Pixel mask ordering.

Bit 4	Description
0	Bit 7 correlates to pixel 7 of a character.
1	Bit 7 correlates to pixel 0 of a character.

Bit	Description
7-5	Reserved.

Default: 0

3DF Foreground Color Register Index = 31 R/W

Bit	Description
7-0	Foreground color register. These 8 bits define the foreground color in color expansion mode.

3DF Background Color Register Index = 32 R/W

Bit	Description
7-0	Background color register. These 8 bits define the background color in color expansion mode.

3DF Color Pattern Register **Index = 33** **R/W**

Bit	Description
7-0	Color pattern register. These bits select the foreground and background color patterns in color expansion mode. When a bit value is 1, the foreground color is selected. Background color is selected when a bit value is 0. Bit 7 corresponds to the first pixel.

3DF Pixel Mask Register **Index = 34** **R/W**

Bit	Description
7-0	Pixel mask bits.

Bit 7-0	Description
0	Mask pixel data.
1	Pass through pixel data.

These bits are effective when NR30[3] =1. For Oak packed pixel modes, this register can be used to mask individual pixels of a character, with bit 0 being the first pixel in a character. For planar modes, this register can be used as the map mask register. In planar mode the least significant 4 bits are used as the map mask bits when the video memory address is odd, and the most significant 4 bits are used when the address is even.

3DF CPU Latch Index Register **Index = 35** **R/W**

Bit	Description
2-0	CPU latch index register. These 3 bits select the CPU latch that will be accessed through the CPU latch data register (index=3DF). This register is automatically incremented when a read from or write to NR36 occurs.
7-3	Reserved.

3DF CPU Latch Data Register **Index = 36** **R/W**

Bit	Description
7-0	CPU latch data register. These 8 bits reflect the data stored in the graphics latch selected by the CPU latch index register.

3DF HC Horizontal Start Register High **Index = 40** **R/W**

Bit	Description
7-0	These are the high order bits of the horizontal starting position of the HC relative to the start of the display area in pixel units. The top left corner is at (0,0).

3DF HC Horizontal Start Register Low **Index = 41** **R/W**

Bit	Description
7-0	These are the low order bits of the horizontal starting position of the HC relative to the start of the display area in pixel units. The top left corner is at (0,0).

3DF HC Vertical Start Register High Index = 42 R/W

Bit	Description
7-0	These are the high order bits of the vertical starting position of the HC relative to the start of the display area in pixel units. The top left corner is at (0,0).

3DF HC Vertical Start Register Low Index = 43 R/W

Bit	Description
7-0	These are the low order bits of the vertical starting position of the HC relative to the start of the display area in pixel units. The top left corner is at (0,0).

3DF HC Horizontal Preset Register Index = 44 R/W

Bit	Description
7-0	This register defines the starting horizontal position of the HC within the 64x64 pixel area. The HC always ends at position 63 (i.e., no wrapping).

3DF HC Vertical Preset Register Index = 45 R/W

Bit	Description
7-0	This register defines the starting vertical position of the HC within the 64x64 pixel area. The HC always ends at position 63 (i.e., no wrapping).

3DF HC Start Address High Low Register Index = 47 R/W

Bit	Description
7-0	This register is the low order byte of the high order word of the linear starting address of the 64x64 pixel buffer within the video memory.

3DF HC Start Address Low High Register Index = 48 R/W

Bit	Description
7-0	This is the high order byte of the low order word of the linear starting address of the 64x64 pixel buffer within the video memory.

3DF HC Start Address Low Low Register Index 49 R/W

Bit	Description
7-0	This is the low order byte of the low order word of the linear start address of the 64x64 pixel buffer within the video memory.

3DF HC Color 0 Register **Index = 4A** **R/W**

Bit	Description
7-0	This register defines the sprite color 0.

3DF HC Color 1 Register **Index = 4B** **R/W**

Bit	Description
7-0	This register defines the sprite color 1.

3DF HC Control Register **Index 4C** **R/W**

Bit	Description
0	HC color control. Power-on default is 0.

Bit 0	Description
0	Disable HC color.
1	Enable HC color.

1 HC display selection.

Bit 1	Description
0	HC is in overscan mode.
1	HC is displayed over the overscan.

2 HC data format.

Bit 2	Description
0	Bit 0 is the first pixel.
1	Bit 7 is the first pixel.

3 HC blink rate enable.

Bit 3	Description
0	Disable HC blinking.
1	Enable HC blinking.

5-4 HC blink rate control.

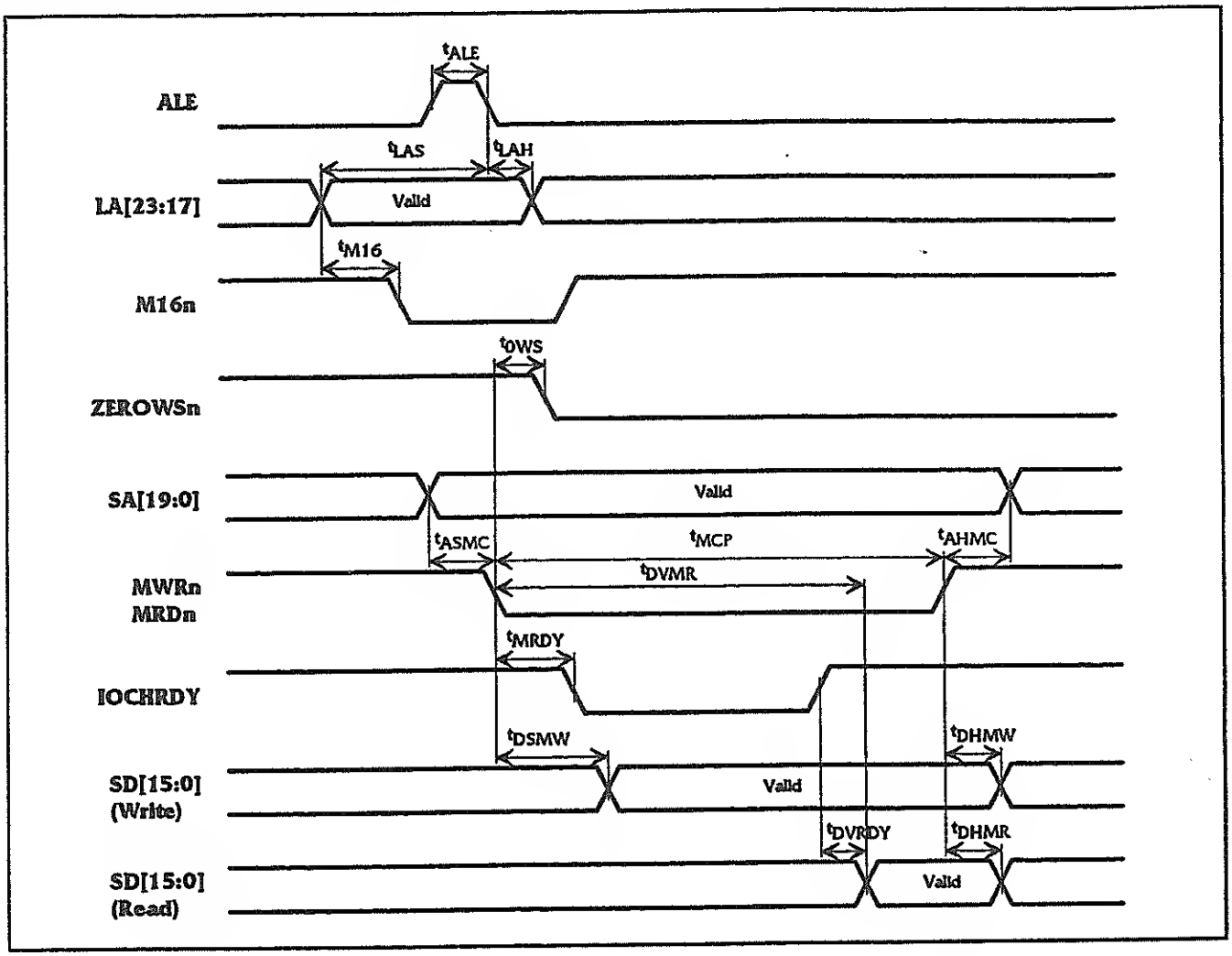
Bits 5.4	Blinking rate
0 0	4 frames on and off.
0 1	8 frames on and off.
1 0	16 frames on and off.
1 1	32 frames on and off.

7-6 Reserved.

Default: 10

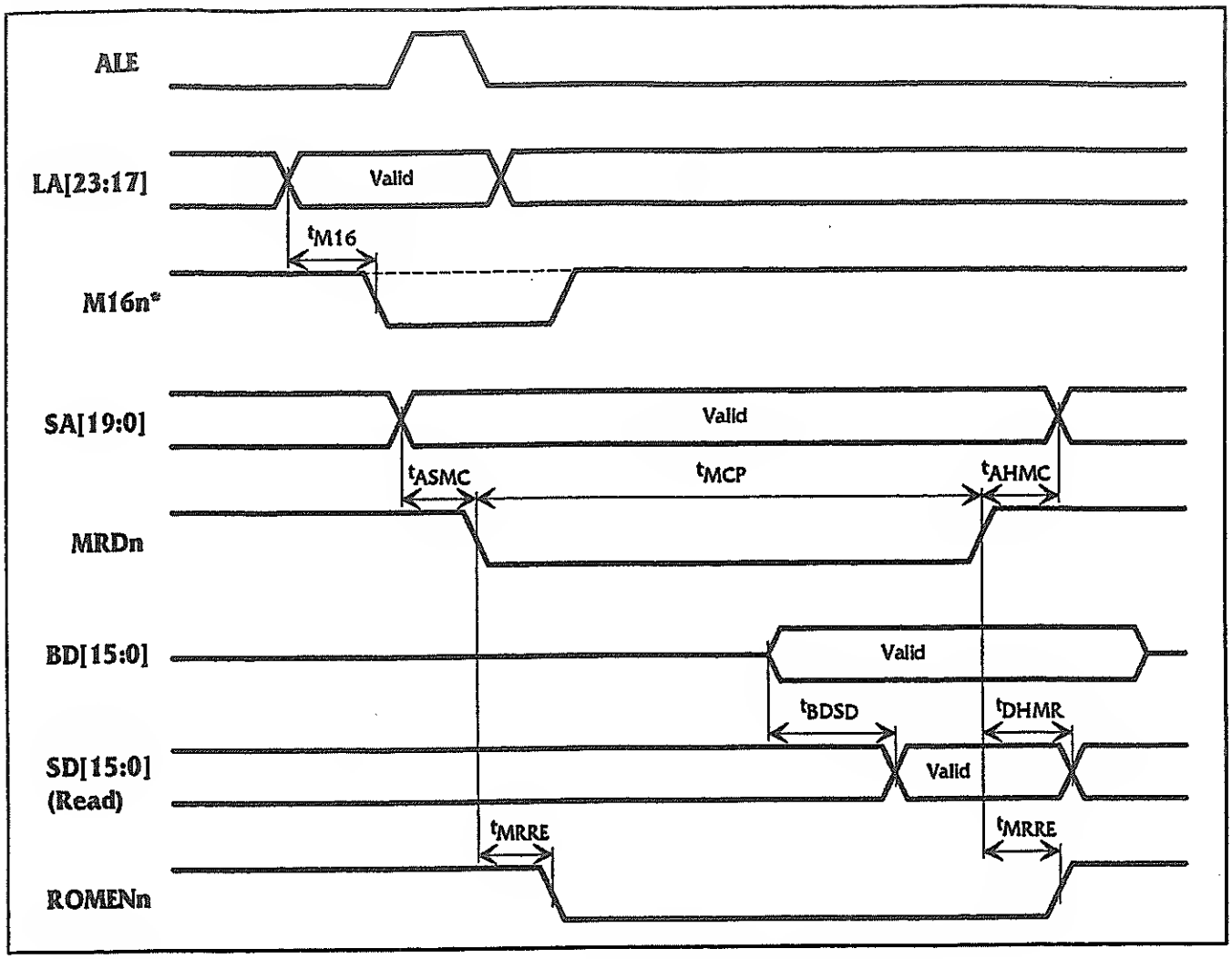
Signal Timing

Video Memory Cycle Timing



Symbol	Parameter	Min (ns)	Max (ns)
tALE	ALE Active to Inactive	40	
tLAS	LA[23:17] Setup to Falling Edge of ALE	15	
tLAH	LA[23:17] Hold from Falling Edge of ALE	5	
tM16	M16n Active from Valid LA[23:17]		40
tOWS	ZEROWSn Delay from Command		25
tASMC	SA[16:0] Setup to Memory Command Active	25	
tMCP	Memory Command Pulse Width	165	
tAHMC	SA[16:0] Hold from Memory Command Inactive	20	
tDVMR	Read Data Valid from MRDn Active (0 Wait State)		65
tMRDY	RDY Inactive from Memory Command Active		30
tDSMW	Write Data Setup to MWn Active	-45	
tDHMW	Write Data Hold from MWn Inactive	15	
tDVRDY	Read Data Valid from RDY Active		5
tDHMR	Read Data Hold from MRDn Inactive	0	

Video ROM Cycle Timing

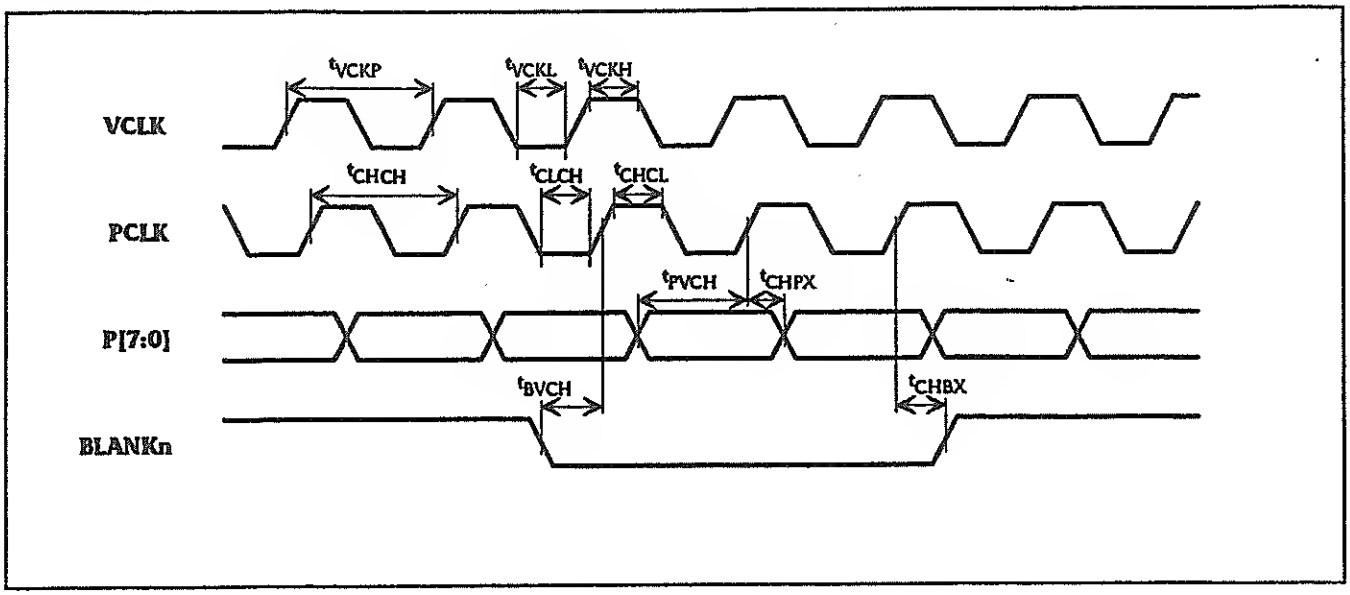


* M16n remains high when the Bus Control Register bit 4 or Configuration Register 1 bit 0 is set to 0.

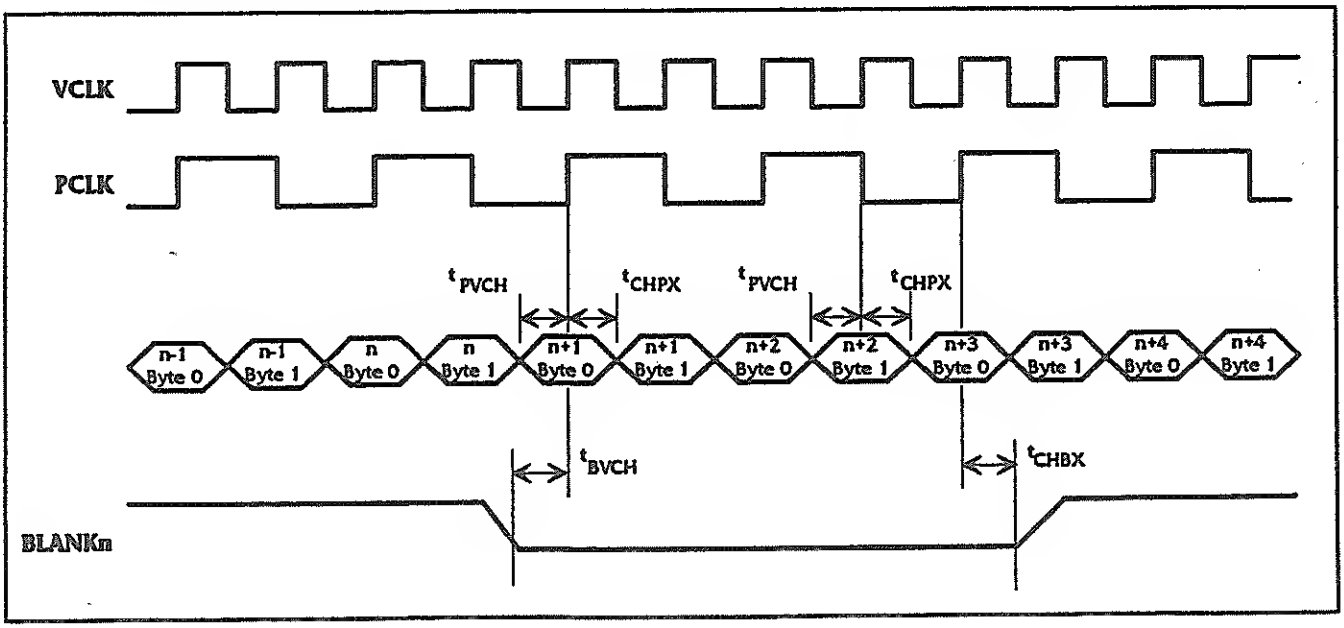
Symbol	Parameter	Min (ns)	Max (ns)
tM16	M16n Active from Valid LA[23:17]		40
tASMC	SA[16:0] Setup to Memory Command Active	25	
tMCP	Memory Command Pulse Width	165	
tAHMC	SA[16:0] Hold from Memory Command Inactive	20	
tDHMW	Write Data Hold from MWRn Inactive	15	
tDHMR	Read Data Hold from MRDn Inactive	0	
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35
tMRRE	ROMENLn Delay from MRDn		25

Video Pixel Timing

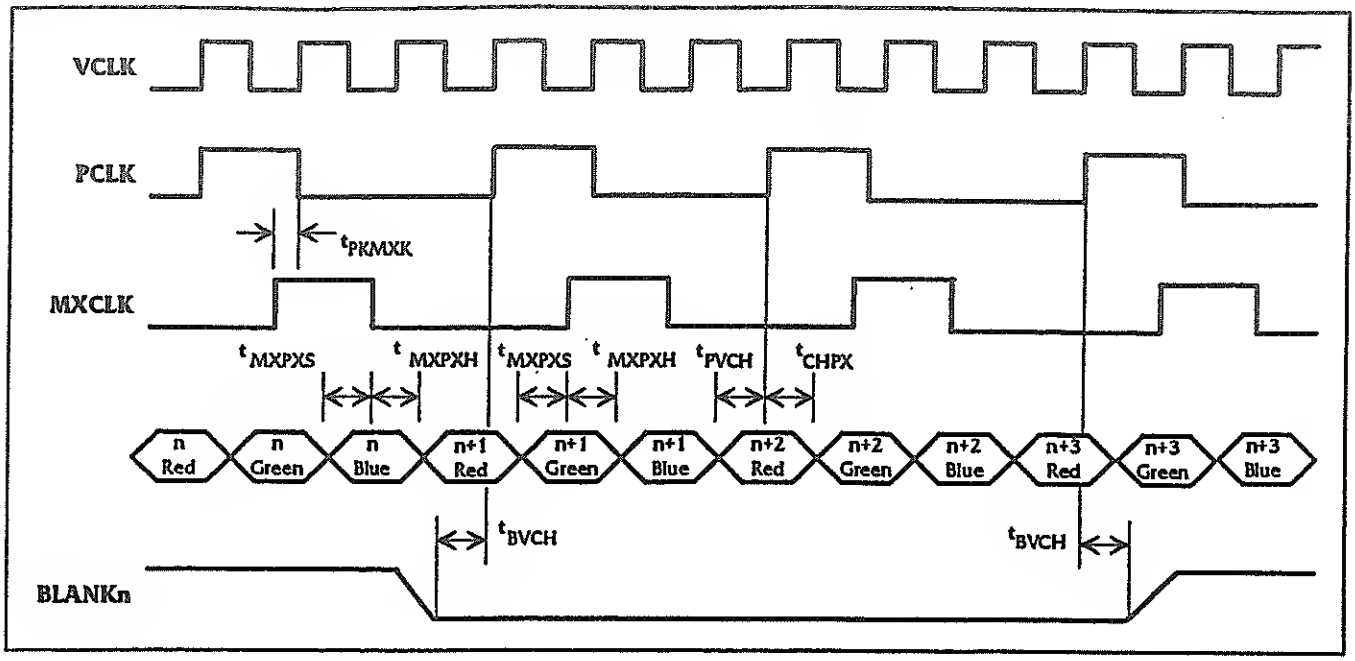
Type 0 DAC



Type 1 DAC -15/16 Bit Color



Type 1 & Type 2 DAC - True Color

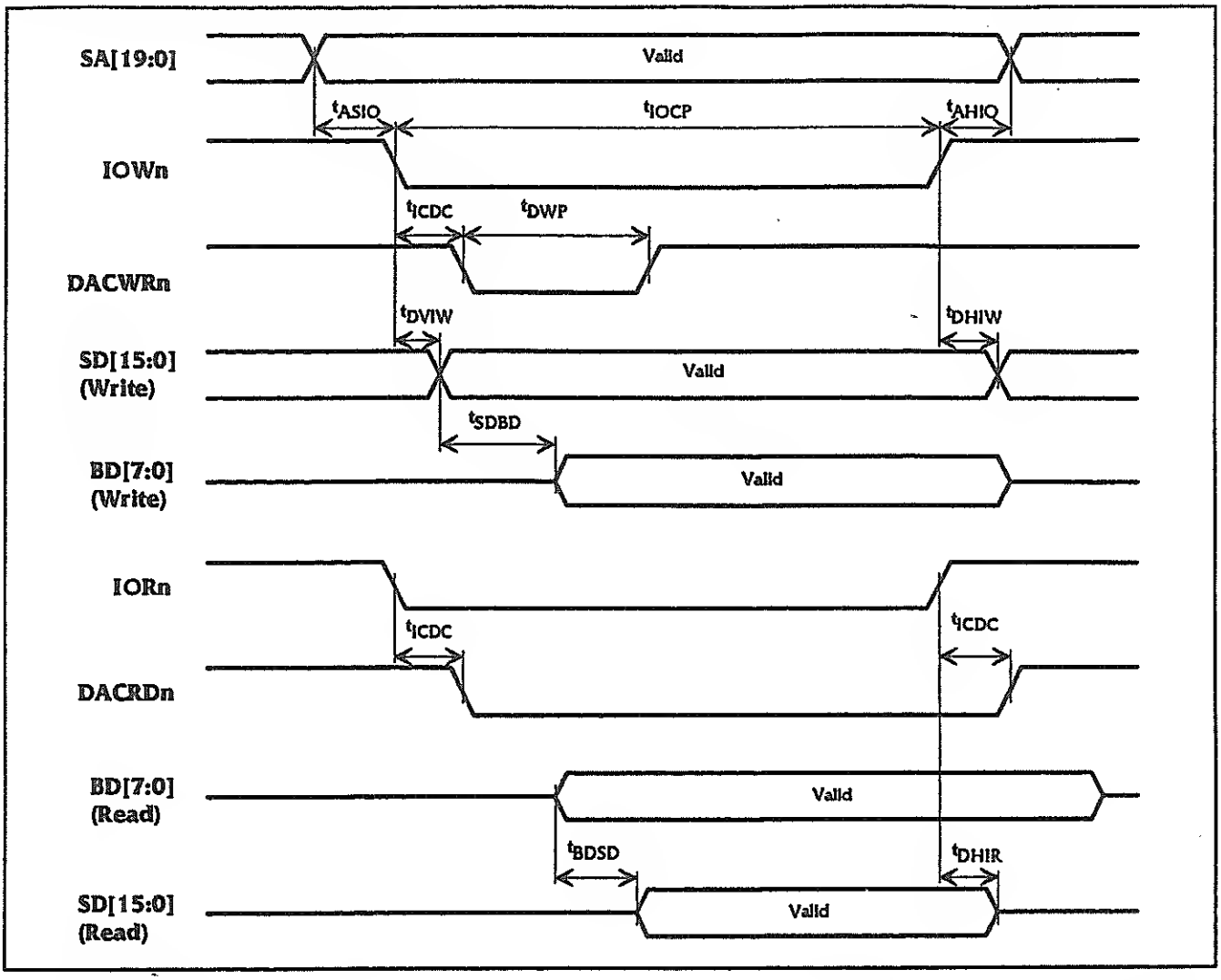


Video Pixel Timing

Type 0, Type 1 and Type 2 DAC Timing

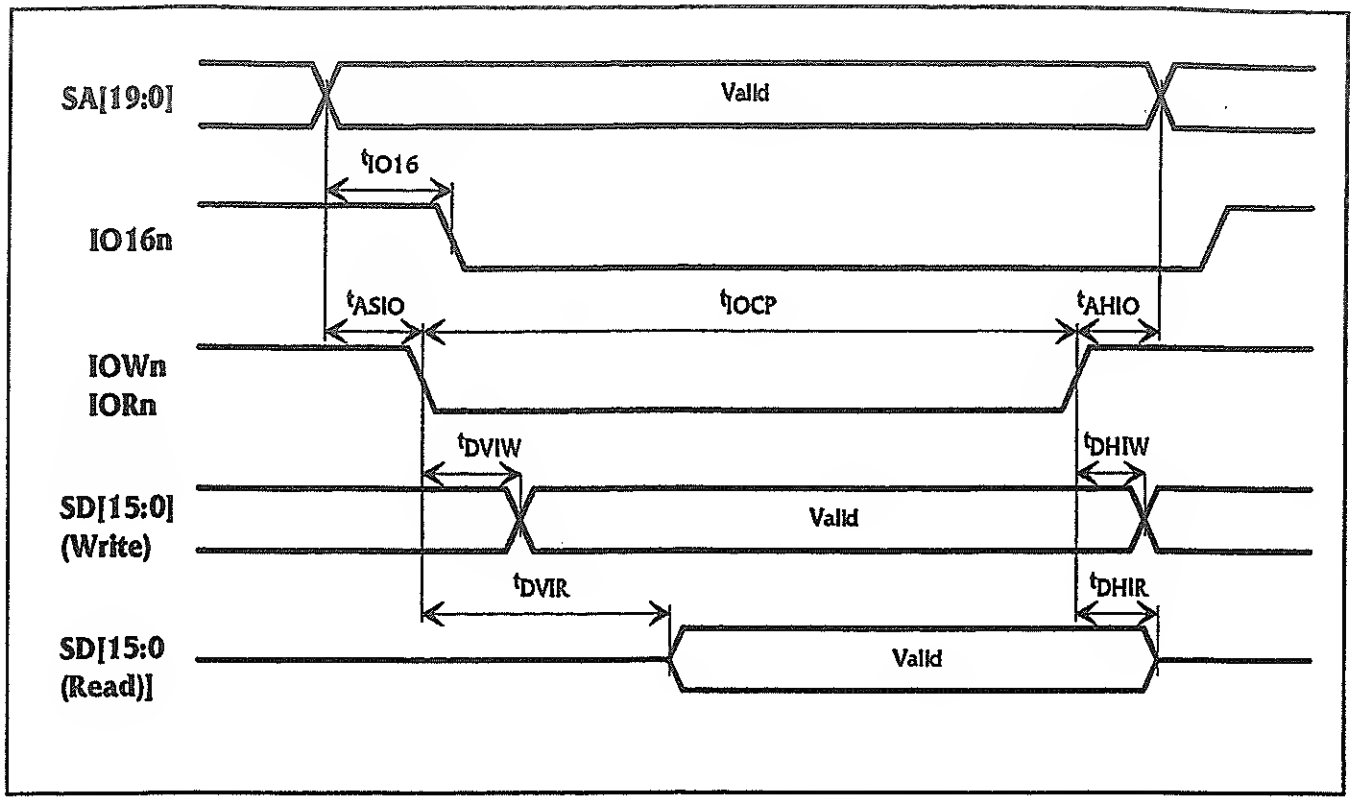
Symbol	Parameter	Min (ns)	Max (ns)
tVCKP	Video Input Clock Period	12	
tVCKH	VCLK Width High	6	
tVCKL	VCLK Width Low	6	
tCHCH	Pixel Clock Period	12	
tCHCL	PCLK Width High	tVCKH-1	
tCLCH	PCLK Width Low	tVCKL-1	
tPVCH	Pixel Word Setup Time	3	
tCHPX	Pixel Word Hold Time	3	
tBVCH	Blankn Setup Time	3	
tCHBX	Blankn Hold Time	3	
tMXPXS	Mux Clock Setup Time	3	
tMXPXH	Mux Clock Hold Time	3	
tPKMXK	Pixel Clock to Mux Clock Delay	2	

Video DAC I/O Timing



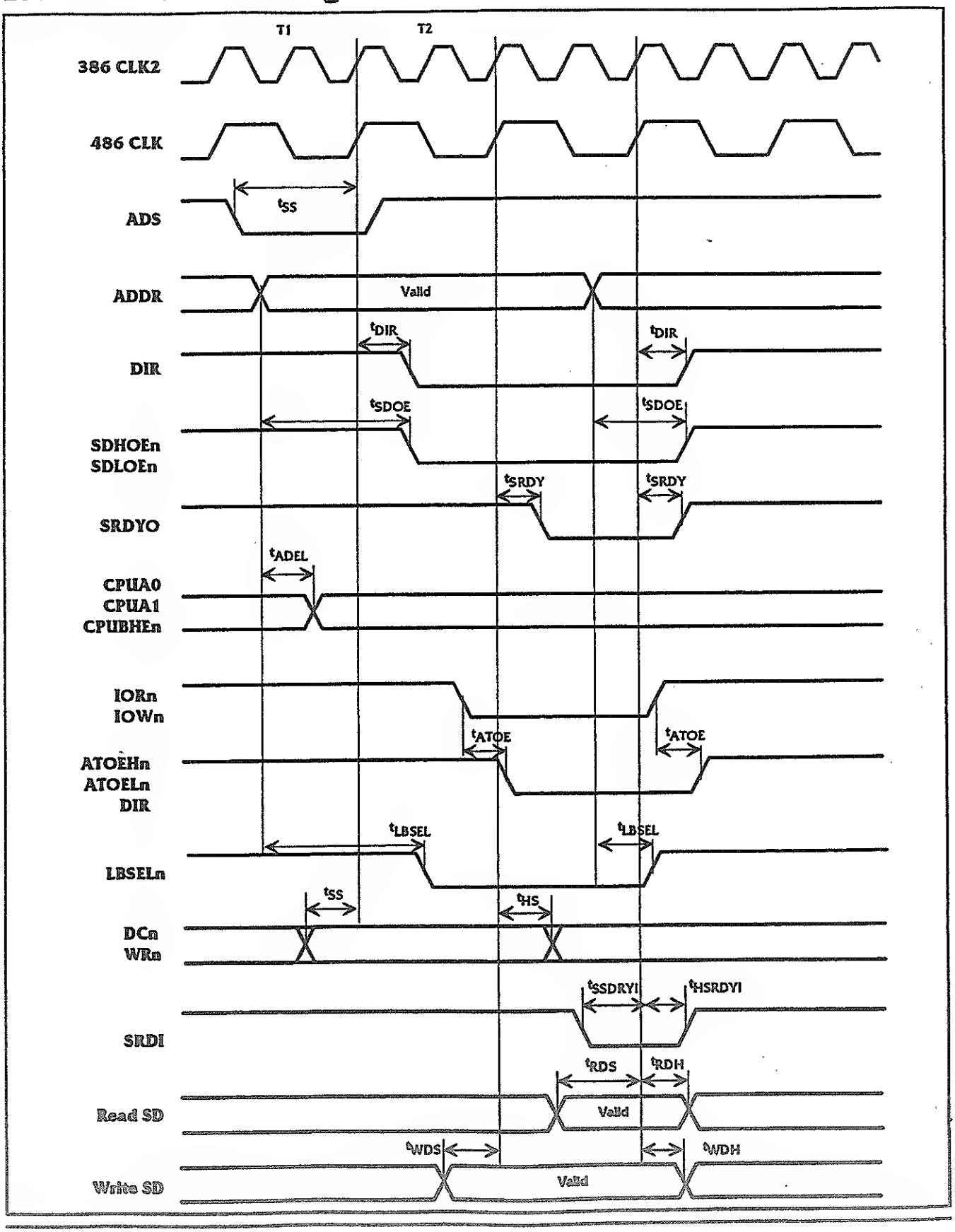
Symbol	Parameter	Min (ns)	Max (ns)
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Setup from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	-55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDHIR	Read Data Hold from IORn Inactive	0	
tICDC	DAC Command Delay from I/O Command		25
tDWP	DACWRn Pulse Width	70	
tSDBD	SD[7:0] Valid to BD[7:0] Valid		50
tBDSD	BD[7:0] Valid to SD[15:0] Valid		35

Video I/O Access Timing



Symbol	Parameter	Min (ns)	Max (ns)
tIO16	IO16n Active from Valid SA[15:0]		60
tASIO	SA[16:0] Setup to I/O Command Active	25	
tAHIO	SA[16:0] Hold from I/O Command Inactive	30	
tIOCP	I/O Command Pulse Width	115	
tDVIW	Write Data Valid from IOWn Active	-55	
tDHIW	Write Data Hold from IOWn Inactive	15	
tDVIR	Read Data Valid from IORn Active		70
tDHIR	Read Data Hold from IORn Inactive	0	

Local Bus Interface Timing



Local Bus Interface Timing

Symbol	Parameter	Min (ns)	Max (ns)
tDIR	DIR Active from CPUCLK	6	25
tSDOE	SDHOEn, SDLOEn Active from Valid Address	6	15
tSRDY	SRDYn Active/Inactive from CPUCLK	6	15
tADEL	CPU A0, A1, BHEn Valid from BE0-3n		see Note 1
tATOE	ATOE Active from IOWRn/IORDn		20
tLBSEL	LBSELn Valid from SA		15
tSSRDYI	SRDYI Setup Time	5	
tHSRDYI	SRDYI Hold Time	3	
tSS	Status Setup Time	4	
tHS	Status Hold Time	4	
tRDS	Read Data Setup Time	12	
tRDH	Read Data Hold Time	7	
tWDS	Write Data Setup Time	7	
tWDH	Write Data Hold Time	5	

Note 1: This delay depends on the necessary external PAL. Please refer to the tables below for PAL speed requirements.

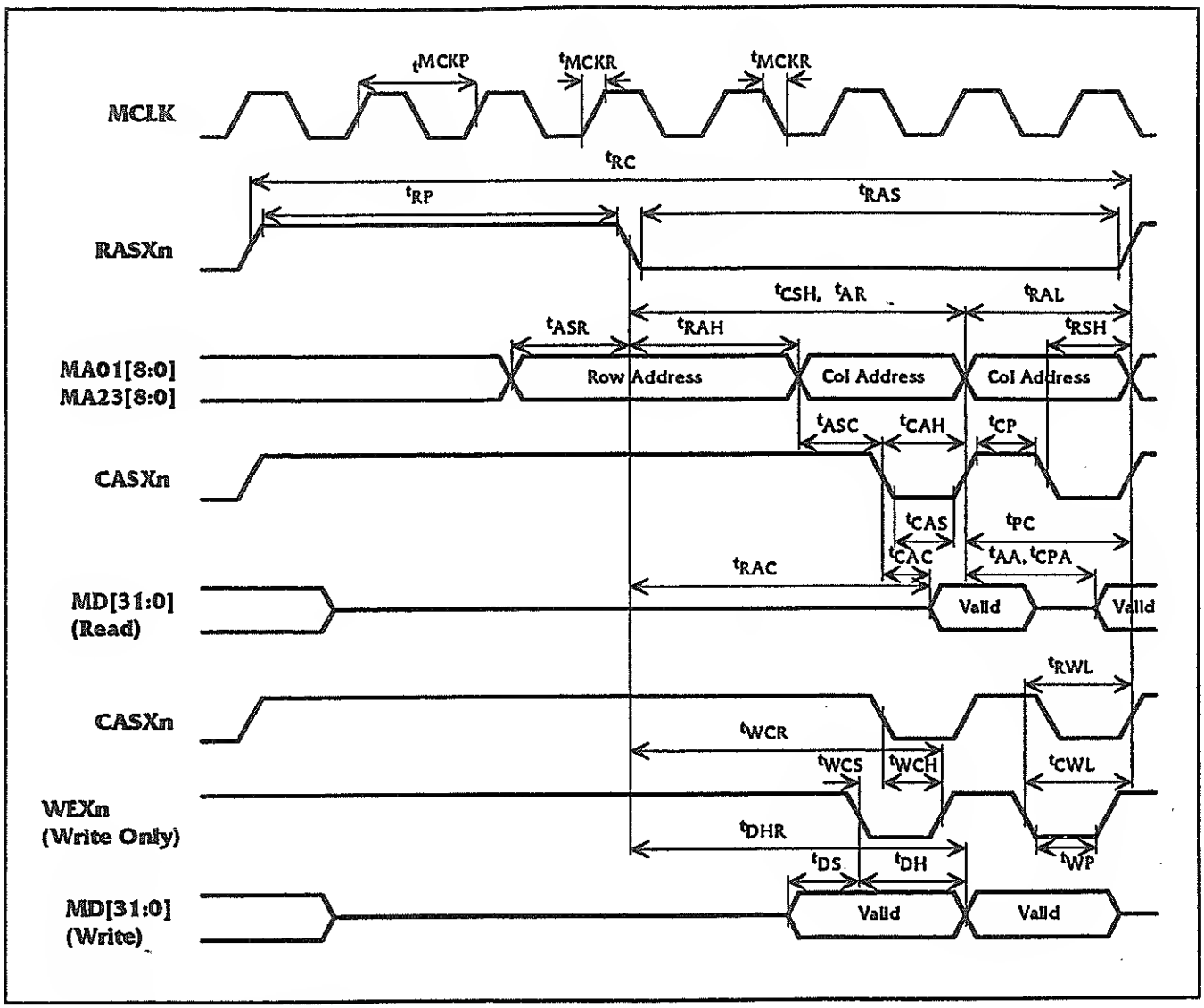
PAL Interface for 80386DX CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns
40 MHz	7 ns

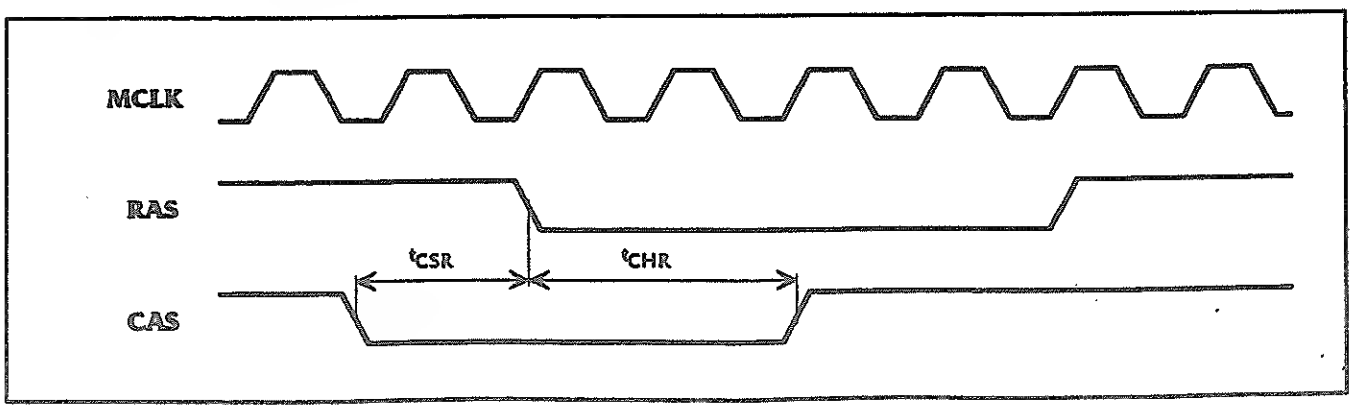
PAL Interface for 80486 CPU

Local Bus Frequency	PAL 16L8
20 MHz	15 ns
25 MHz	15 ns
33 MHz	10 ns

DRAM Interface Timing



Memory Refresh Timing



DRAM Interface Timing & Memory Refresh Timing

SYMBOL	PARAMETER	Min (ns)	Max (ns)
tMP	Memory Clock Period	22	25
tMCKR	Memory Clock Rise/Fall		2.5
tRC	Random Rd/Wr Cycle Time	7tMP	
tRP	RASn Precharge Time	3tMP	
tRAS	RASn Pulse Width	4tMP	
tCSH	CASn Hold Referenced to RASn	4tMP	
tAR	Column Address Hold Ref. to RASn	4tMP	
tRAL	Column Address to RASn Lead Time	2tMP	
tASR	Row Address Setup Time	1tMP	
tRAH	Row Address Hold Time	1tMP	
tRSH	RASn Hold Referenced to CASn	1tMP	
tASC	Column Address Setup Time	1tMP	
tCAH	Column Address Hold Time	1tMP	
tCP	CASn Precharge Time	1tMP	
tCAS	CASn Pulse Width	1tMP	
tPC	Fast Page Mode Cycle Time	2tMP	
tRAC	Access Time from RASn		4tMP
tCAC	Access Time from CASn		1tMP
tAA	Access Time from Col. Addr. (MA)		2tMP
tCPA	Access Time from CASn Precharge		2tMP
tRWL	WExxn to RASn Lead Time	1tMP	
tWCR	WExxn Hold Ref. to RA5n	4tMP	
tWCS	WExxn Setup to CASn	0tMP	
tWCH	WExxn Hold Ref. to CASn	1tMP	
tCWL	WExxn to CASn Lead Time	1tMP	
tWP	WExxn Pulse Width	1tMP	
tDHR	MD Hold Ref. to RASn	4tMP	
tDS	MD Setup to WExxn	1tMP	
tDH	MD Hold to WExxn	1tMP	
tCSR	CASn Setup to RASn (Ref. Cycle) (2)	1tMP	
tCHR	CASn Hold to RASn (Ref. Cycle) (2)	2tMP	

Notes:

1. Refresh Cycles are implemented as CASn before RASn REFRESH cycles.
2. Write cycles are implemented as EARLY WRITE cycles.

DC Specification

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to +7.0V

Stresses above those listed may cause permanent damage to the OTI-087. These specifications are stress ratings only and do not apply to operational use. Functional operation of this device at these or any other conditions above those indicated in this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: T_A=0°C to 70°C, V_{DD}=5V +/-5%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Conditions
Voh	Output Voltage High	2.4		V	Ioh=400 uA
Vol	Output Voltage Low		.4	V	Iol=24 mA, Note 1,2
Vol	Output Voltage Low		.4	V	Iol=12 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=10 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=8 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=4 mA, Note 1
Vol	Output Voltage Low		.4	V	Iol=2 mA, Note 1
Vih	Input Voltage High	2	VCC+0.5	V	TTL, Note 3
Vil	Input Voltage Low	-0.5	0.8	V	TTL, Note 3
Ili	Input Leakage Current	-10	10	uA	
Oli	Output Leakage Current	-10	10	uA	
ICC	Operating Supply Current		125	mA	
CI	Input Capacitance		8	pF	
Co	Output Capacitance		8	pF	
Clo	I/O Capacitance		8	pF	

Notes:

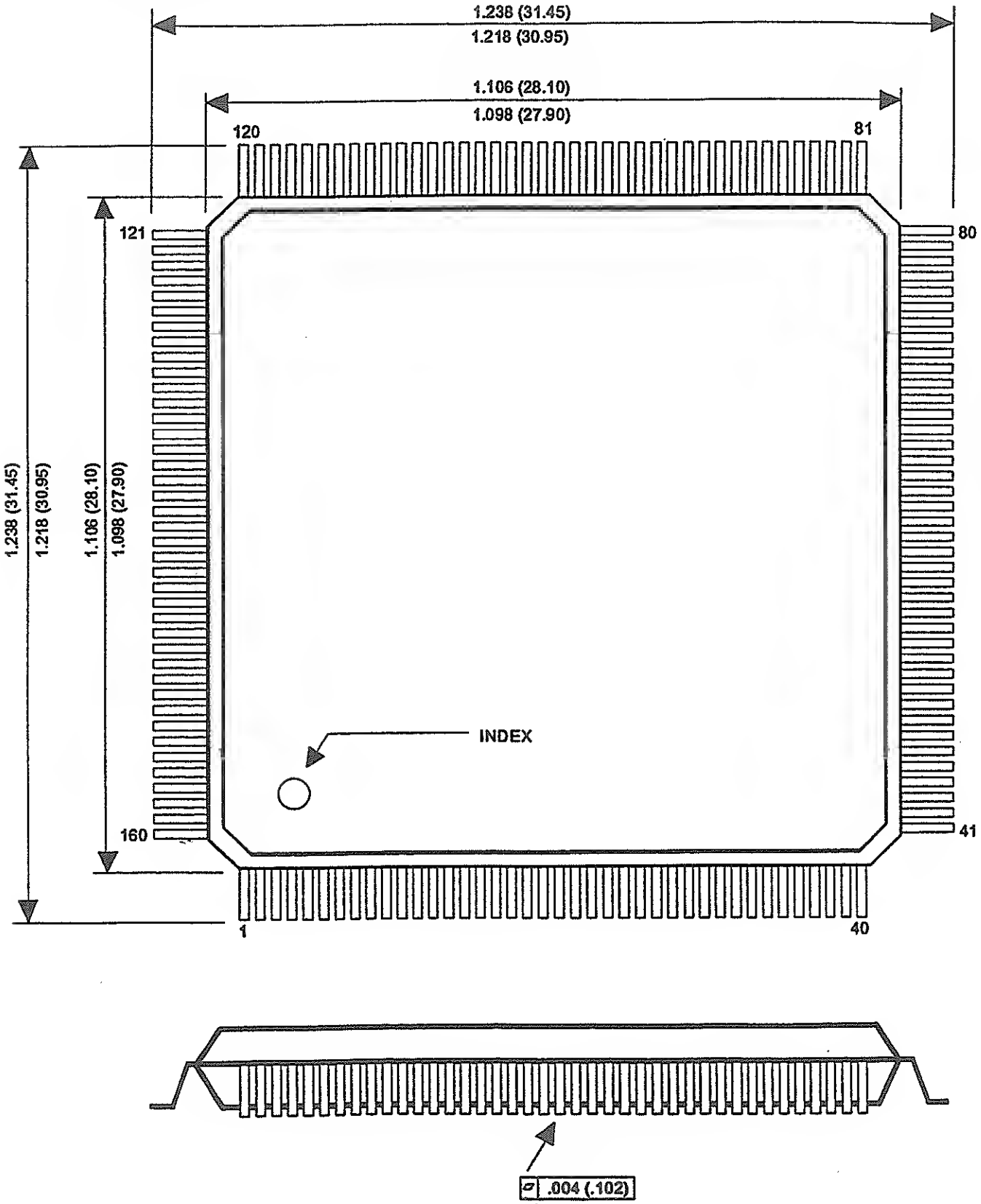
1) Output Current (Iol) Capabilities:
   - 24mA: SD[15:0] with slew control.
   - 8mA: SRDY, RASLn, RASHn, CASAn, WEAn, WEBn, MA01[0], MA23[0], HSYNC, VSYNC, LBSELn, BLANKn, P[7:0], PCLK
   - 4mA: BD[7:0], MA01[8:1], MA23[8:1], MD[31:0]
   - 2mA: CSEL[3:0], DACRn, RACWn, ROMENLn

2) Open Drain (open collector) Outputs:
   - 24mA: IOCHRDY, CINTn, IO16n, M16n, ZEROWSn

3) Input Structures:
   - TTL: All

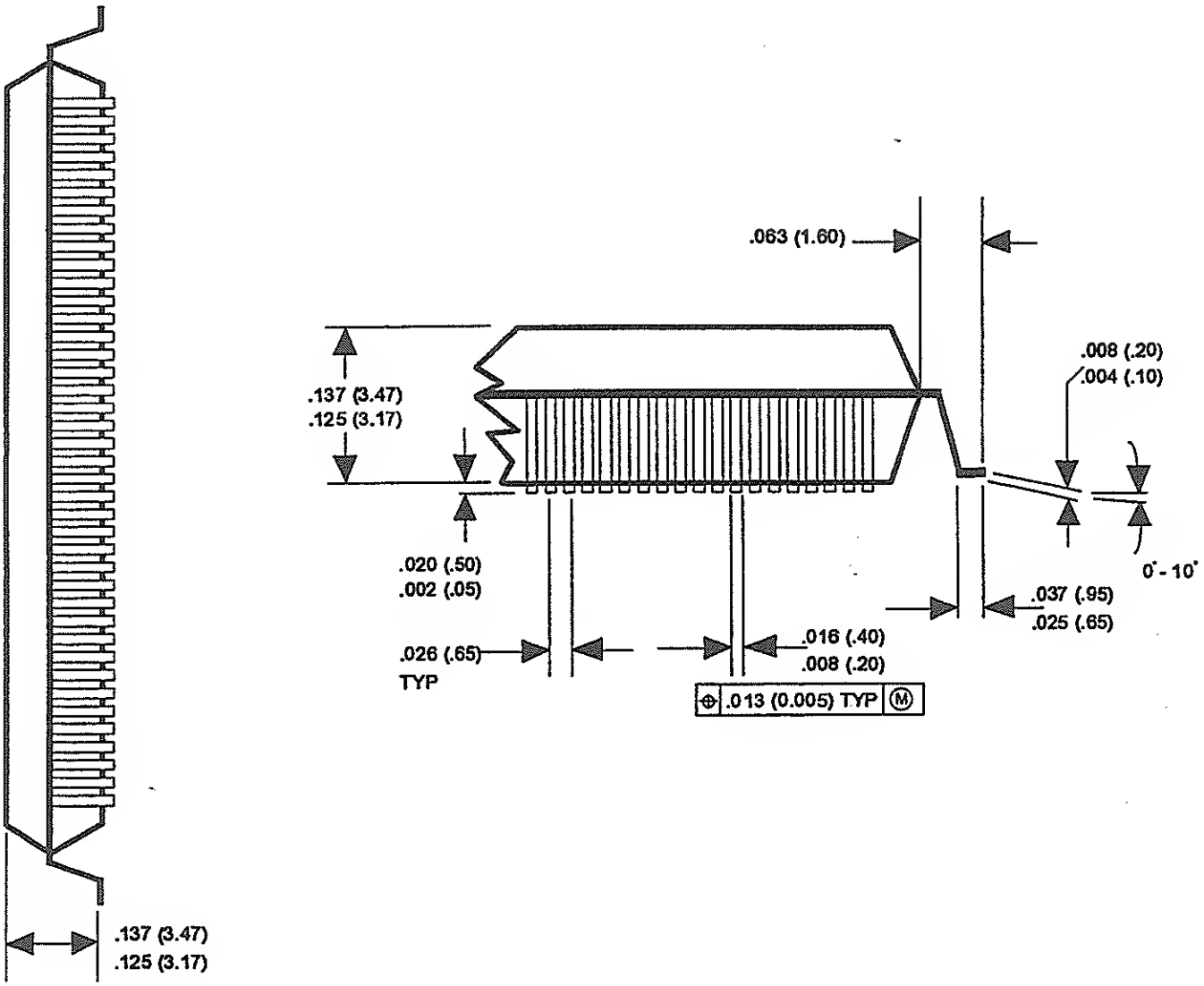
Package Outlines

All dimensions in mils (mm).



Package Outlines

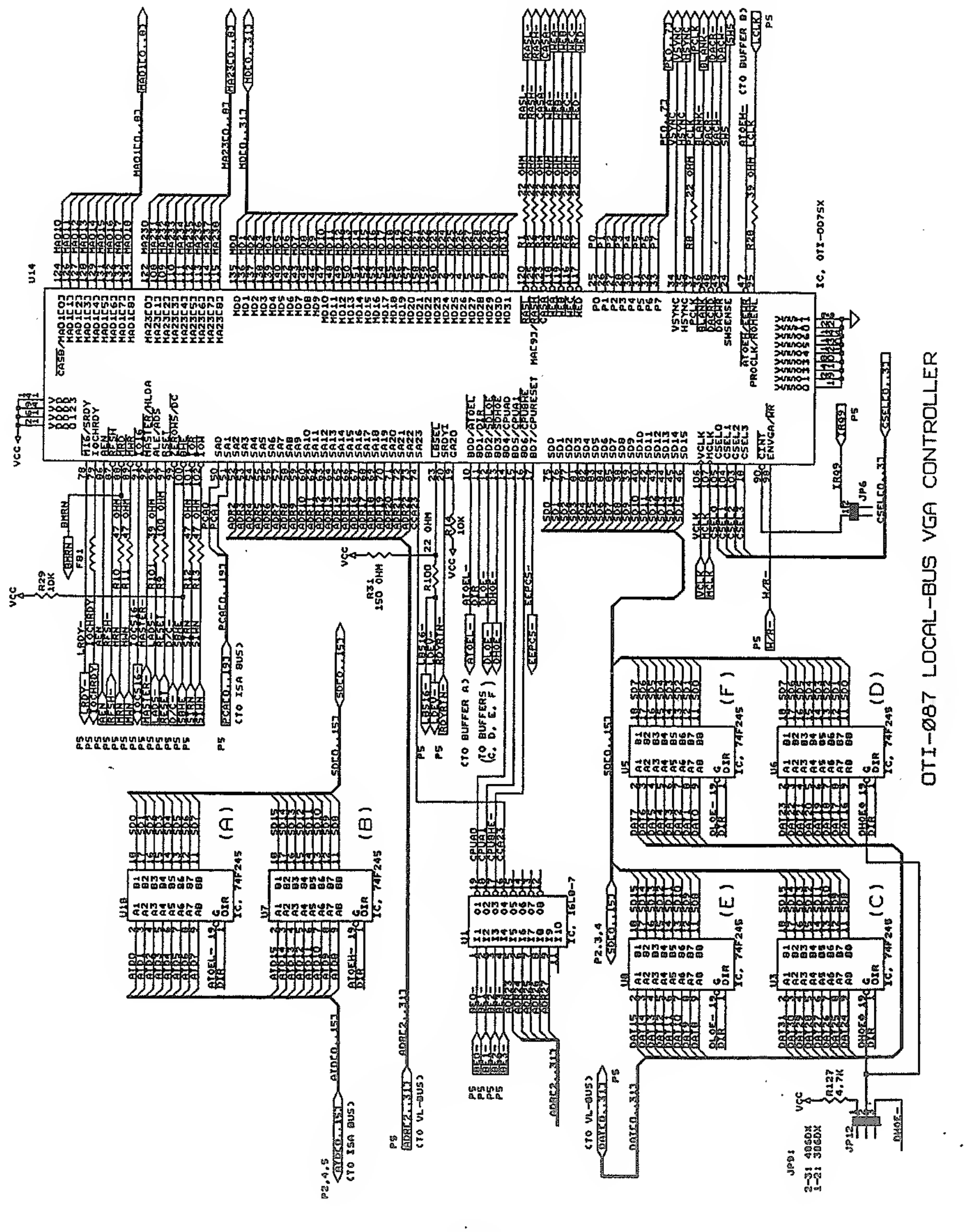
All dimensions in mils (mm).

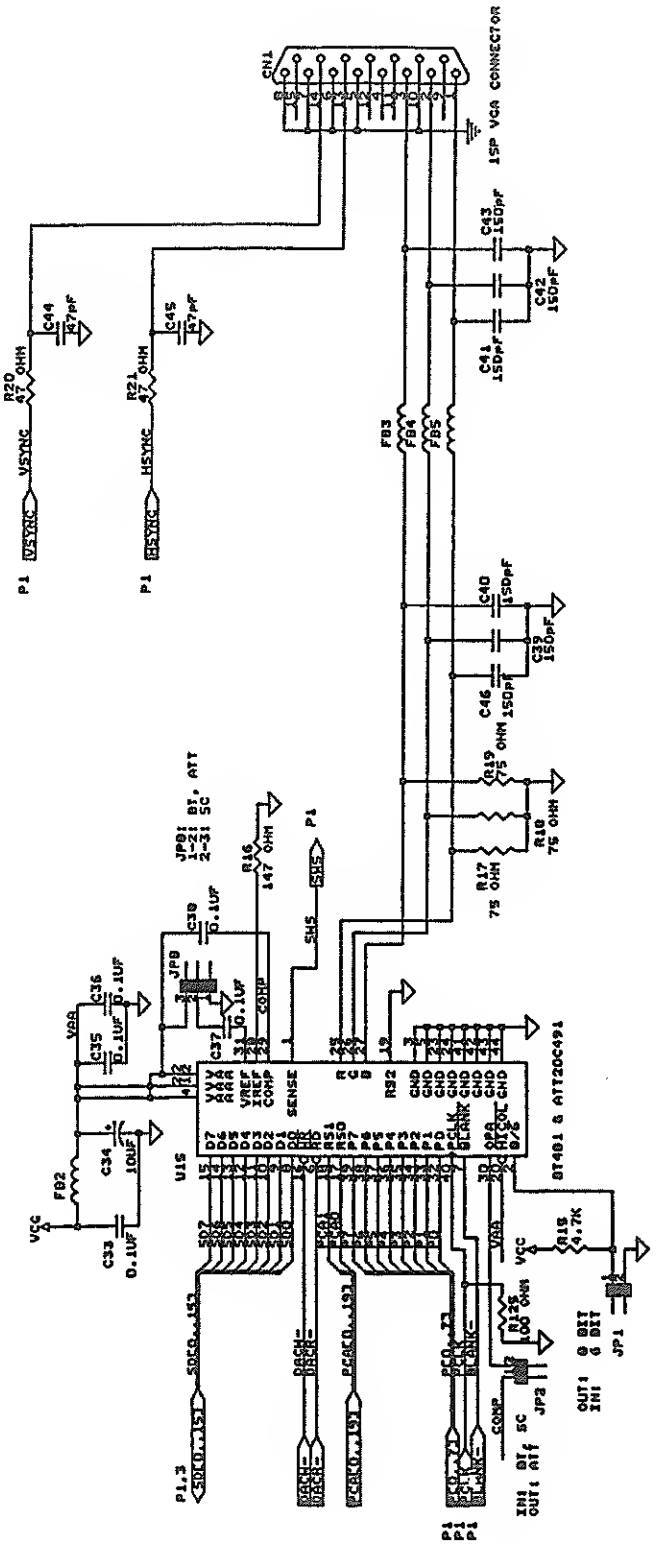


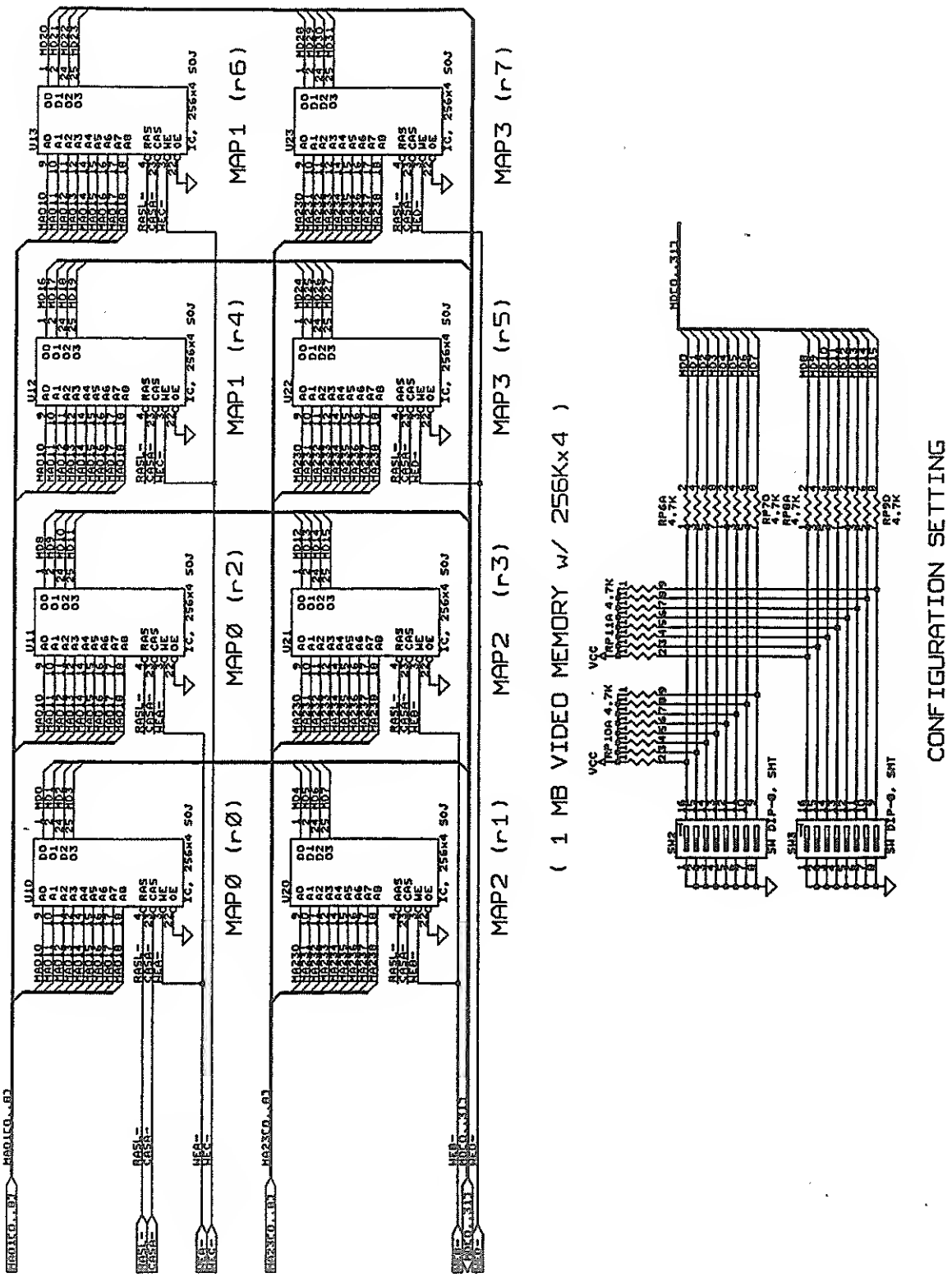
Notes:

1. Controlling dimension is mm.
2. Oak Technology, Inc. reserves the right to change the package dimensions at any time and without notice.

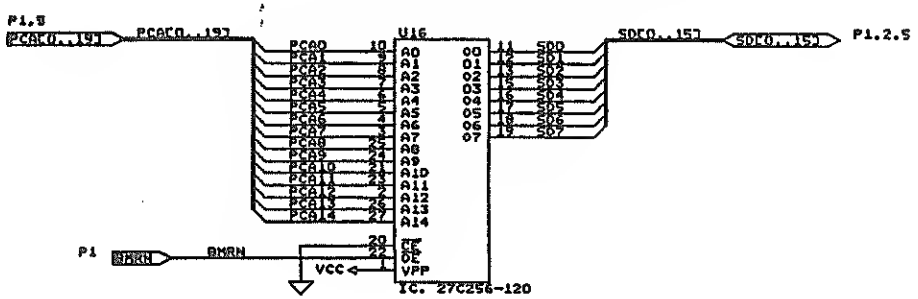
OTI-087 VESA Local Bus Schematics


OTI-087 LOCAL-BUS VGA CONTROLLER


24-BIT TRUE-COLOR/HI COLOR RAMDAC
CN1
15P VGA CONNECTOR
R20 47 OHM
R21 47 OHM
C44 47pF
C45 47pF
VSYNC
HSYNC
C43 150pF
C42 150pF
C41 150pF
FB3
FB4
FB5
C40 150pF
C39 150pF
C46 150pF
R19 75 OHM
R18 75 OHM
R17 75 OHM
JP8: 1-2: BI. ATT
2-3: SC
C38 0.1UF
R16 147 OHM
C36 0.1UF
C35 0.1UF
C37 0.1UF
JP8
C34 10UF
C33 0.1UF
FB2
VCC
VAA
COMP
SENSE
BT481 & ATT20C491
R15 4.7K
R125 100 OHM
JP2
JP1
OUT: 8 BIT
IN: 6 BIT
IN: BI. Att SC
OUT: Att SC

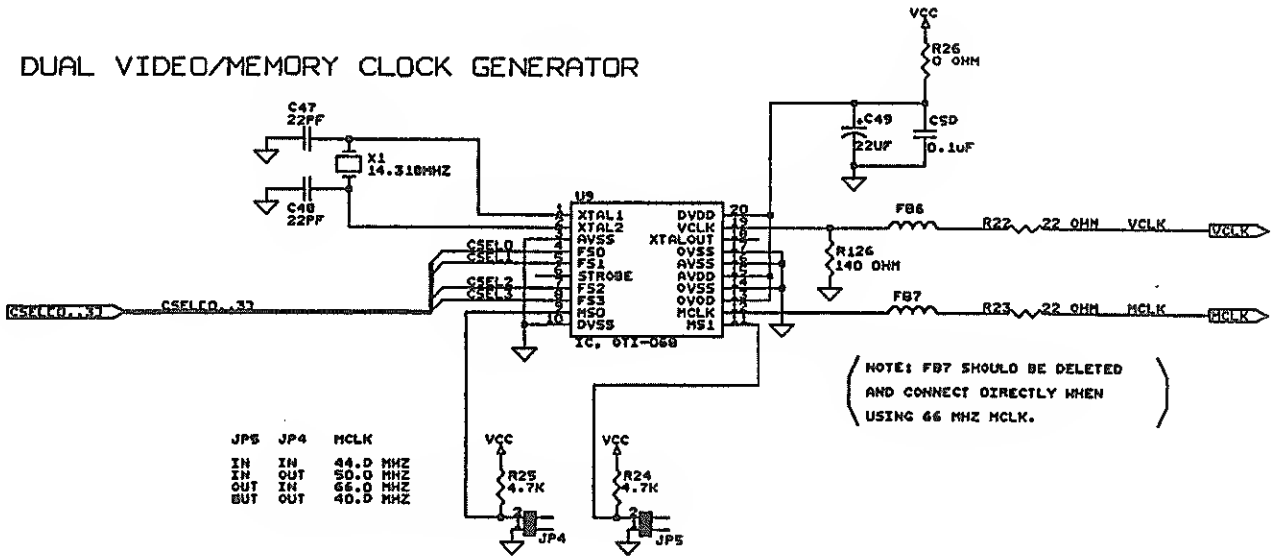

MAP0 (r0)
MAP1 (r4)
MAP1 (r6)
MAP2 (r1)
MAP2 (r3)
MAP3 (r5)
MAP3 (r7)
(1 MB VIDEO MEMORY w/ 256Kx4)
CONFIGURATION SETTING

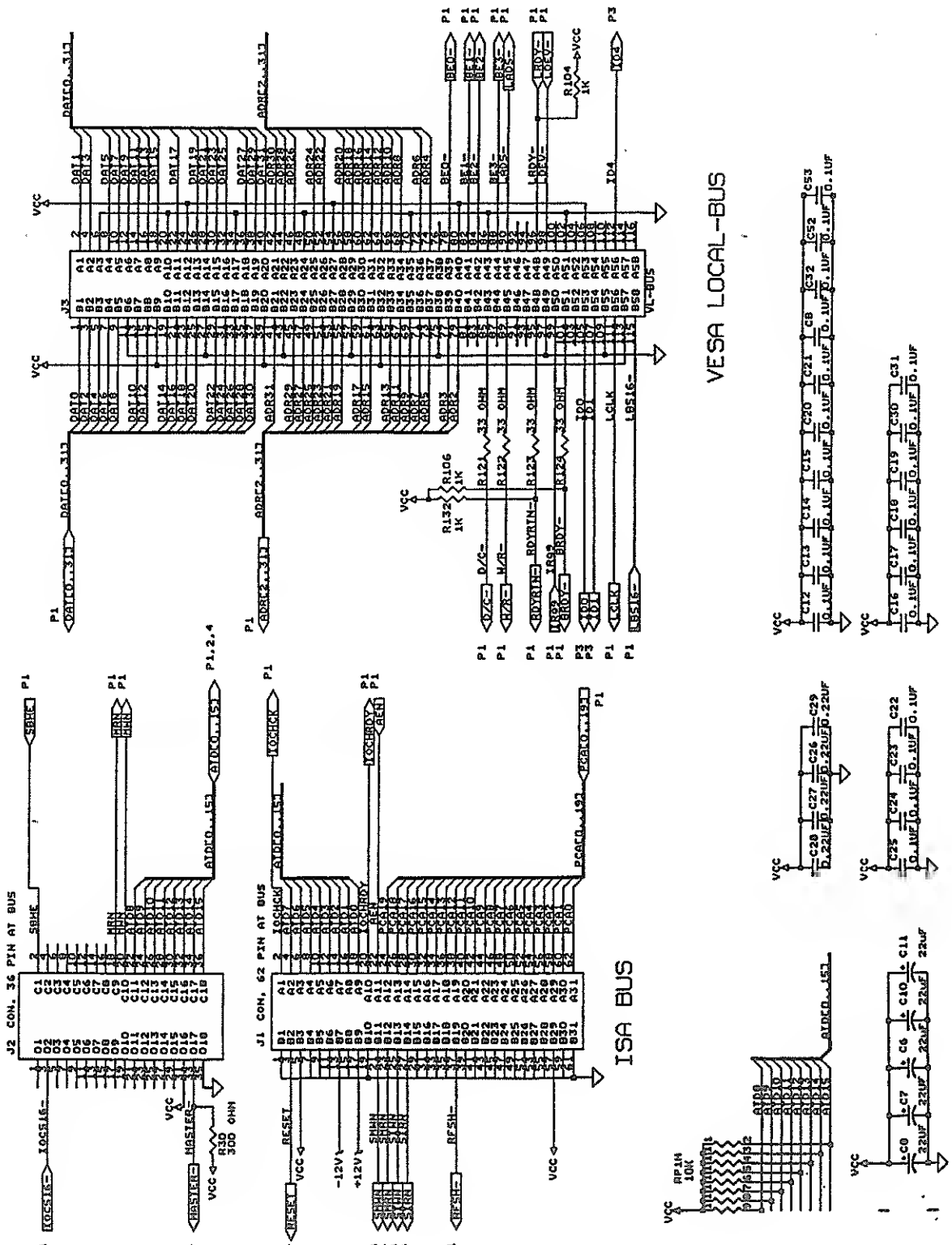
8-BIT VIDEO BIOS (32KB)



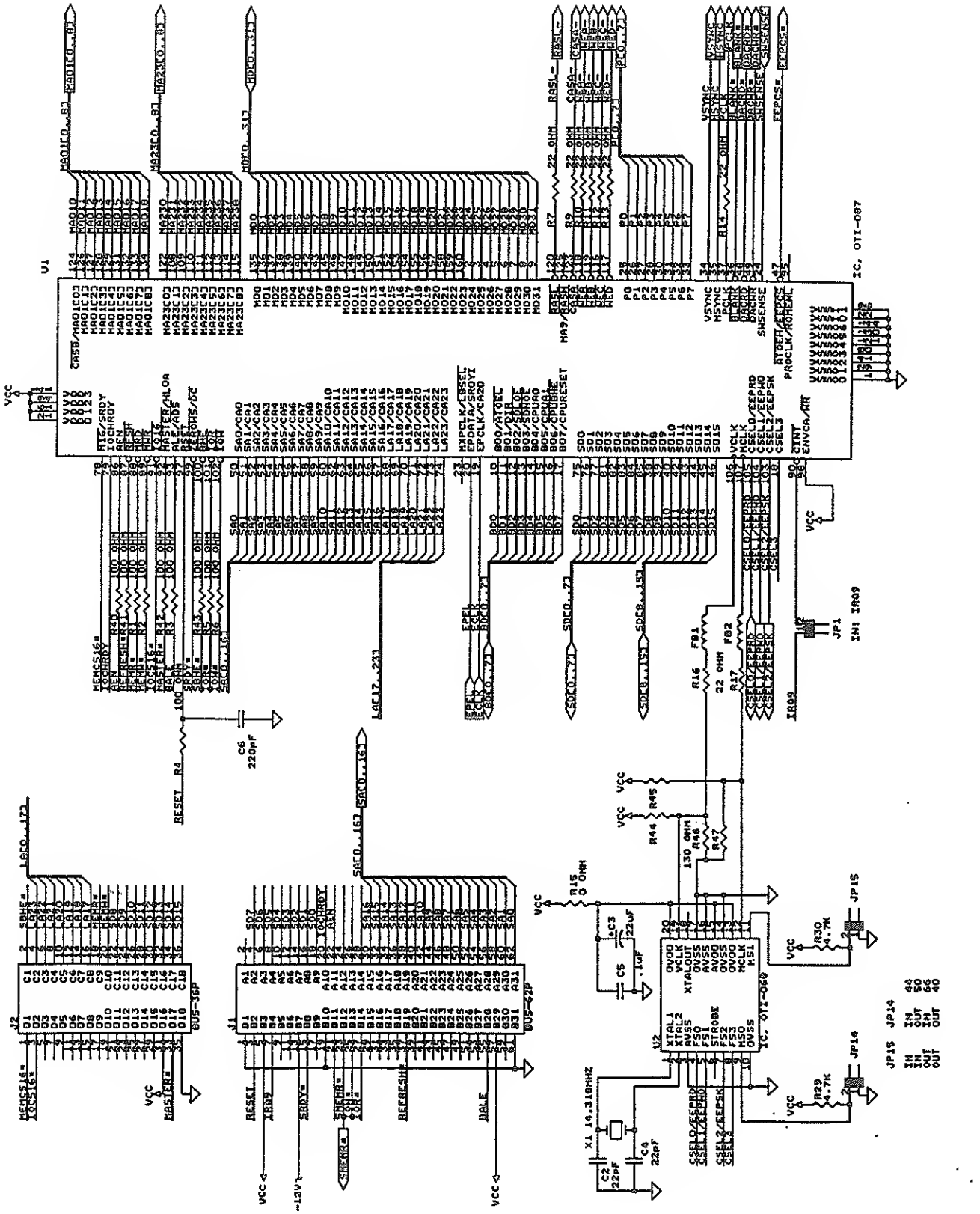
1024-BIT EEPROM

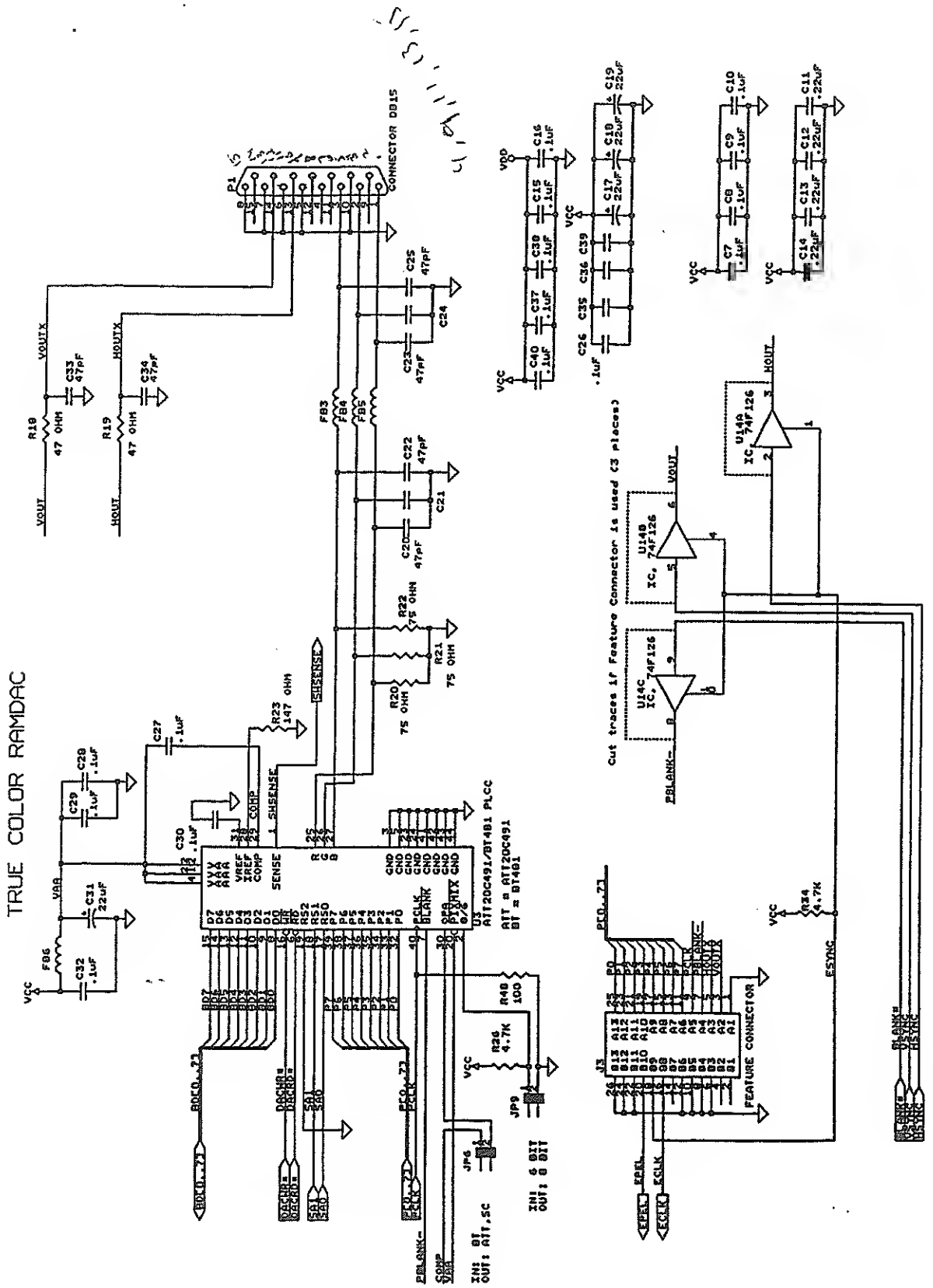
DUAL VIDEO/MEMORY CLOCK GENERATOR

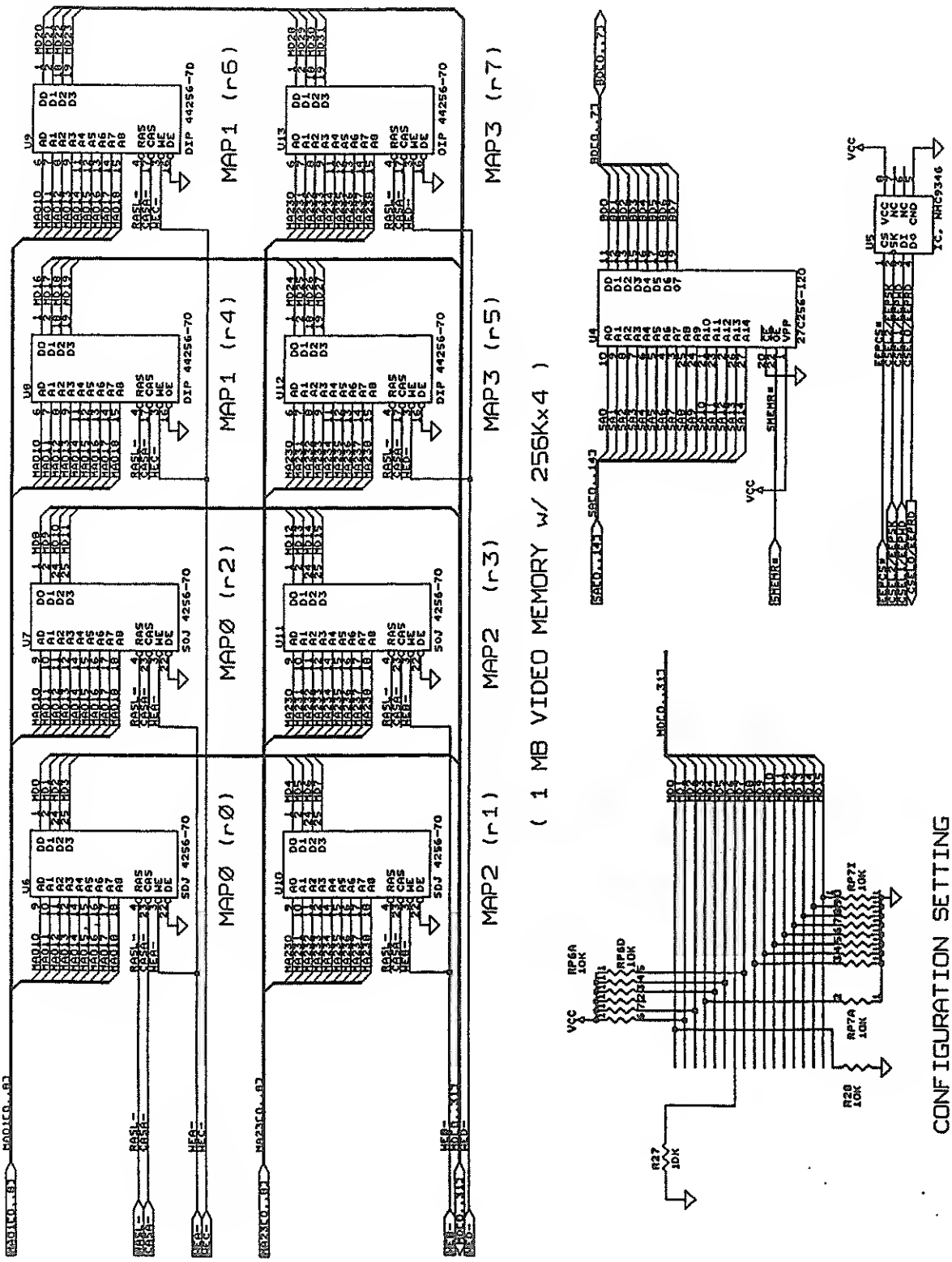



VESA LOCAL-BUS
ISA BUS
J3
VL-BUS
J2 CON. 36 PIN AT BUS
J1 CON. 62 PIN AT BUS
DATA0..31
ADDR2..31
R104 1K
R106 1K
R132 1K
R121 33 OHM
R122 33 OHM
R123 33 OHM
R124 33 OHM
R30 300 OHM
RP1N 10K
C0 32uF
C6 22uF
C7 32uF
C10 22uF
C11 22uF
C12 C13 C14 C15 C20 C21 C8 C32 C52 C53 0.1UF
C16 C17 C18 C19 C30 C31 0.1UF
C22 C23 C24 C25 0.1UF
C26 C27 C28 C29 0.22UF
VCC
P1
P3

OTI-087 True Color ISA-Bus Schematics




TRUE COLOR RAMDAC
CONNECTOR DB15
P1
VOUTX
HOUTX
R18 47 OHM
R19 47 OHM
C33 47pF
C34 47pF
C25 47pF
C24
C23 47pF
C22 47pF
C21
C20 47pF
FB3
FB4
FB5
R22 75 OHM
R21 75 OHM
R20 75 OHM
R23 147 OHM
SHSENSE
C27 .1uF
C28 .1uF
C29 .1uF
C30 .1uF
C31 22uF
C32 .1uF
FB6
VAA
VCC
VREF
COMP
I_SHSENSE
SENSE
RSET
U3
ATT20C491/BT481 PLCC
ATT = ATT20C491
BT = BT481
CLK
BLANK
SYNC
P7-0
R48 100
R26 4.7K
JP9
JP6
IN: 6 BIT
OUT: 8 BIT
IN: 8I
OUT: ATT,SC
PBLANK-
COMP
VAA
C16 .1uF
C15 .1uF
C30 .1uF
C37 .1uF
C40 .1uF
C19 22uF
C18 22uF
C17 22uF
C36
C39
C35
C26 .1uF
C10 .1uF
C9 .1uF
C8 .1uF
C7 .1uF
C11 .22uF
C12 .22uF
C13 .22uF
C14 .22uF
VDD
VCC
U14A 74F126
U14B 74F126
U14C 74F126
IC
HOUT
VOUT
Cut traces if Feature Connector is used (3 places)
R34 4.7K
ESYNC
FEATURE CONNECTOR
J3
PCLK
PBLANK
VOUTX
HOUTX
EPEL
ECLK
BLANK*
VSYNC
HSYNC


(1 MB VIDEO MEMORY w/ 256Kx4)
MAP0 (r0)
MAP0 (r2)
MAP1 (r4)
MAP1 (r6)
MAP2 (r1)
MAP2 (r3)
MAP3 (r5)
MAP3 (r7)
CONFIGURATION SETTING

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